

**RADIATION HARDENED
POWER MOSFET
SURFACE MOUNT (SMD-0.5)**

200V, N-CHANNEL
REF: MIL-PRF-19500/704

R₅ TECHNOLOGY

Product Summary

Part Number	Radiation Level	RDS(on)	I _D	QPL Part Number
IRHNJ57230SE	100 kRads(Si)	0.22Ω	12A	JANSR2N7486U3



Description

IR HiRel R₅ technology provides high performance power MOSFETs for space applications. These devices have been characterized for both Total Dose and Single Event Effect (SEE) with useful performance up to LET of 80 (MeV/(mg/cm²)). The combination of low RDS(on) and low gate charge reduces the power losses in switching applications such as DC-DC converters and motor controllers. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

Features

- Single Event Effect (SEE) Hardened
- Low RDS(on)
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Electrically Isolated
- Ceramic Package
- Light Weight
- Surface Mount
- ESD Rating: Class 1C per MIL-STD-750, Method 1020

Absolute Maximum Ratings

Pre-Irradiation

	Parameter		Units
I _D @ V _{GS} = 12V, T _C = 25°C	Continuous Drain Current	12	A
I _D @ V _{GS} = 12V, T _C = 100°C	Continuous Drain Current	7.8	
I _{DM}	Pulsed Drain Current ①	48	
P _D @ T _C = 25°C	Maximum Power Dissipation	75	W
	Linear Derating Factor	0.6	W/°C
V _{GS}	Gate-to-Source Voltage	±20	V
E _{AS}	Single Pulse Avalanche Energy ②	60	mJ
I _{AR}	Avalanche Current ①	12	A
E _{AR}	Repetitive Avalanche Energy ①	7.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.4	V/ns
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (for 5s)	
	Weight	1.0 (Typical)	g

For Footnotes, refer to the page 2.

Electrical Characteristics @ T_J = 25°C (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	200	—	—	V	V _{GS} = 0V, I _D = 1.0mA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.26	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.22	Ω	V _{GS} = 12V, I _D = 7.8A ④
V _{GS(th)}	Gate Threshold Voltage	2.5	—	4.5	V	V _{DS} = V _{GS} , I _D = 1.0mA
G _{fs}	Forward Transconductance	6.0	—	—	S	V _{DS} = 15V, I _D = 7.8A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	10	μA	V _{DS} = 160V, V _{GS} = 0V
		—	—	25		V _{DS} = 160V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -20V
Q _G	Total Gate Charge	—	—	35	nC	I _D = 12A
Q _{GS}	Gate-to-Source Charge	—	—	9.0		V _{DS} = 100V
Q _{GD}	Gate-to-Drain ('Miller') Charge	—	—	15		V _{GS} = 12V
t _{d(on)}	Turn-On Delay Time	—	—	25	ns	V _{DD} = 100V
t _r	Rise Time	—	—	100		I _D = 12A
t _{d(off)}	Turn-Off Delay Time	—	—	35		R _G = 7.5Ω
t _f	Fall Time	—	—	30		V _{GS} = 12V
L _s + L _D	Total Inductance	—	4.0	—	nH	Measured from center of Drain pad to center of Source pad
C _{iss}	Input Capacitance	—	1000	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	184	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	11	—		f = 1.0MHz

Source-Drain Diode Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	12	A	
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	48		
V _{SD}	Diode Forward Voltage	—	—	1.2	V	T _J = 25°C, I _S = 12A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	300	ns	T _J = 25°C, I _F = 12A, V _{DD} ≤ 25V
Q _{rr}	Reverse Recovery Charge	—	—	3.2	μC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S + L _D)				

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	—	1.67	°C/W
R _{θJ-PCB}	Junction-to-PC Board (Soldered to 2" sq copper clad board)	—	6.9	—	

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② V_{DD} = 50V, starting T_J = 25°C, L = 0.82mH, Peak I_L = 12A, V_{GS} = 12V
- ③ I_{SD} ≤ 12A, di/dt ≤ 366A/μs, V_{DD} ≤ 200V, T_J ≤ 150°C
- ④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%
- ⑤ **Total Dose Irradiation with V_{GS} Bias.** 12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
- ⑥ **Total Dose Irradiation with V_{DS} Bias.** 160 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	1000 kRads (Si) ²		Units	Test Conditions
		Min.	Max.		
BV _{DSS}	Drain-to-Source Breakdown Voltage	200	—	V	V _{GS} = 0V, I _D = 1.0mA
V _{GS(th)}	Gate Threshold Voltage	2.0	4.5	V	V _{DS} = V _{GS} , I _D = 1.0mA
I _{GSS}	Gate-to-Source Leakage Forward	—	100	nA	V _{GS} = 20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	-100	nA	V _{GS} = -20V
I _{DSS}	Zero Gate Voltage Drain Current	—	10	μA	V _{DS} = 200V, V _{GS} = 0V
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (TO-3)	—	0.222	Ω	V _{GS} = 12V, I _D = 7.8A
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (SMD-2)	—	0.22	Ω	V _{GS} = 12V, I _D = 7.8A
V _{SD}	Diode Forward Voltage ④	—	1.3	V	V _{GS} = 0V, I _D = 12A

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET (MeV/(mg/cm ²))	Energy (MeV)	Range (μm)	VDS (V)				
			@ VGS = 0V	@ VGS=-5V	@ VGS=-10V	@ VGS =-15V	@ VGS=-20V
38 ± 5%	300 ± 7.5%	38 ± 7.5%	200	200	200	200	200
61 ± 5%	330 ± 7.5%	31 ± 10%	200	200	200	185	120
84 ± 5%	350 ± 7.5%	28 ± 7.5%	200	200	150	50	25

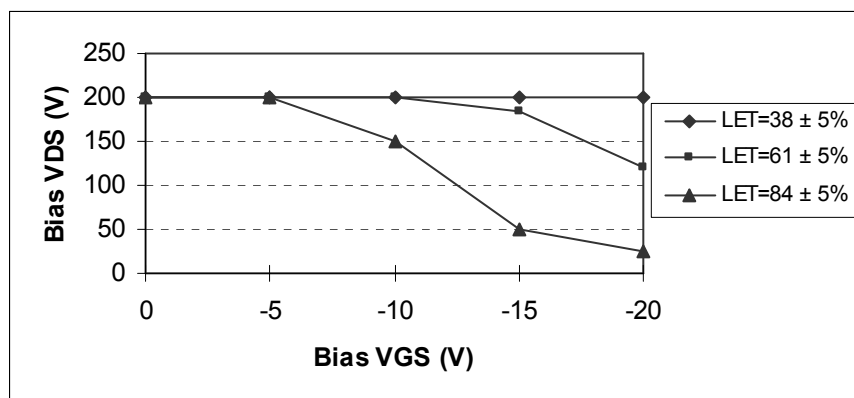
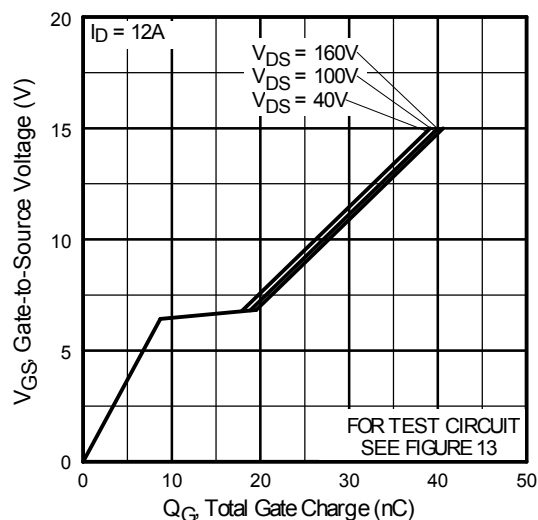
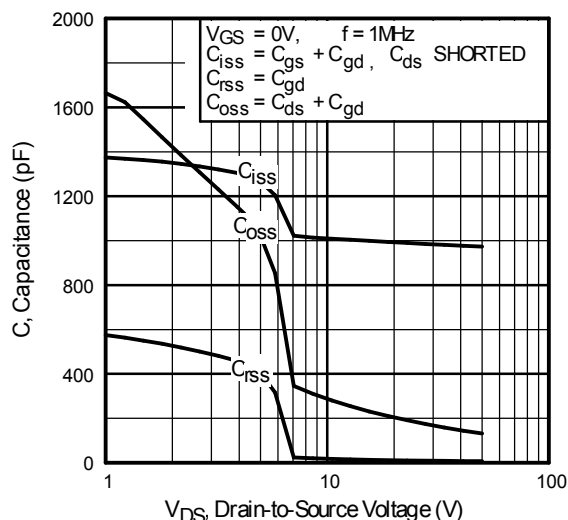
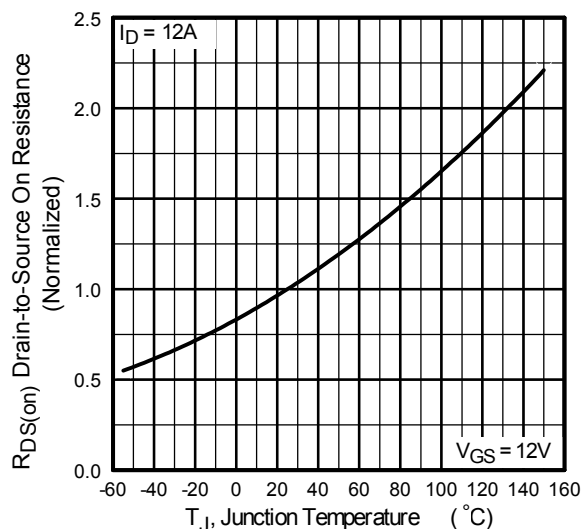
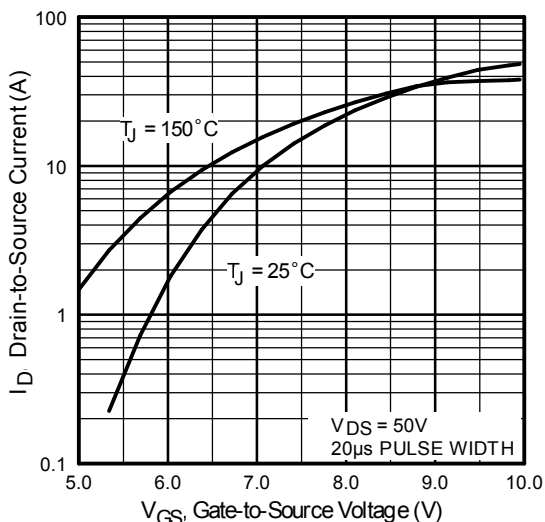
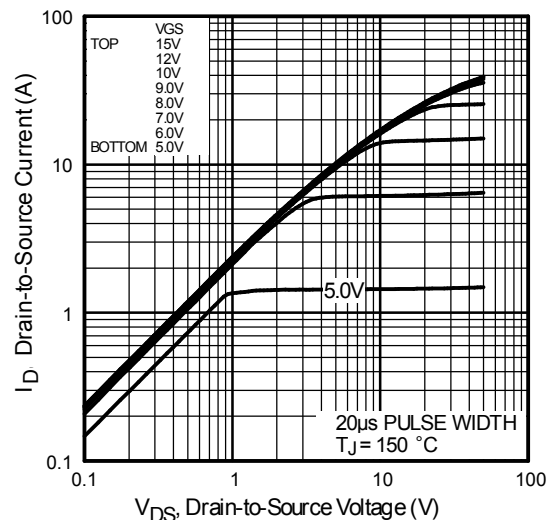
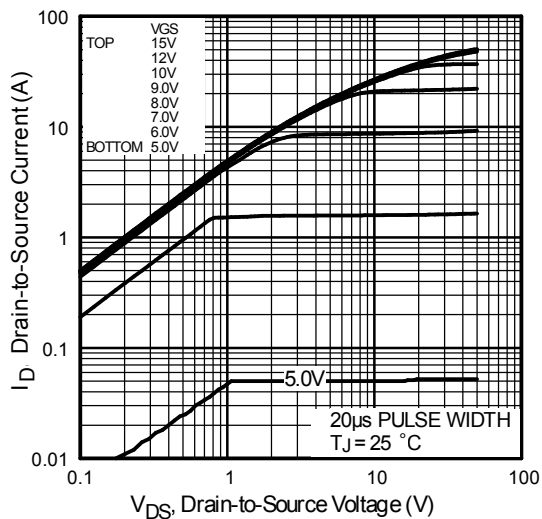


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

Pre-Irradiation



Pre-Irradiation

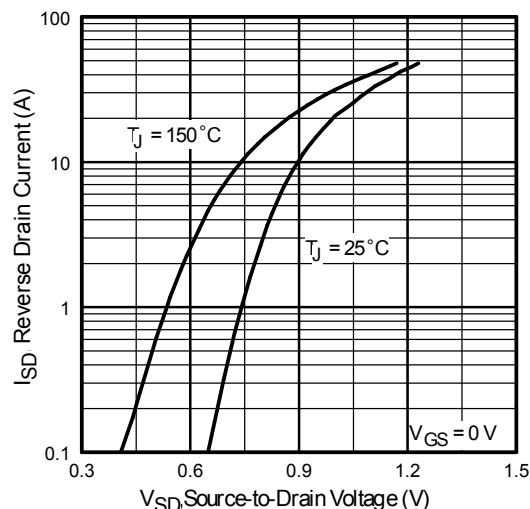


Fig 7. Typical Source-Drain Diode Forward Voltage

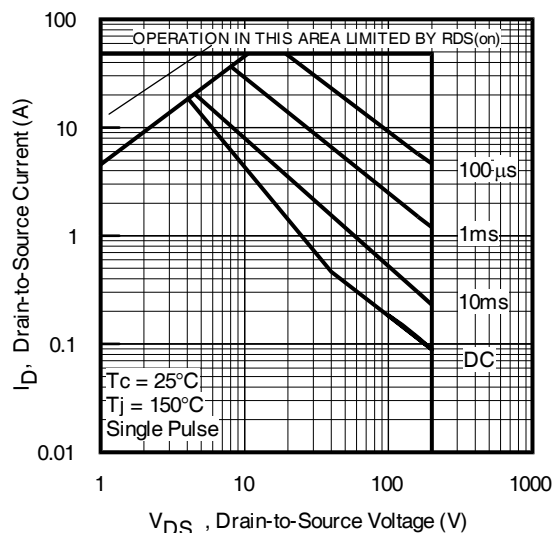


Fig 8. Maximum Safe Operating Area

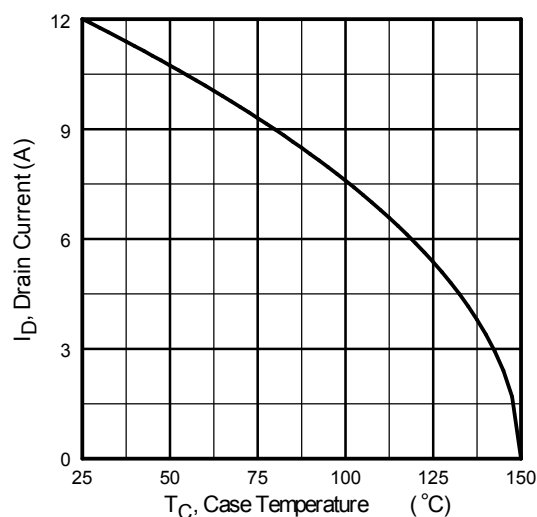


Fig 9. Maximum Drain Current Vs. Case Temperature

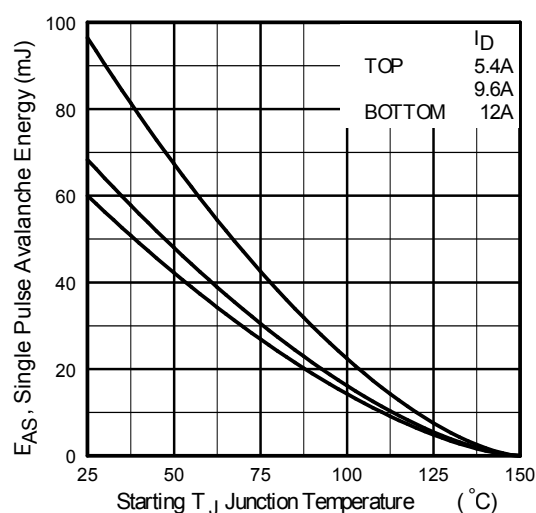


Fig 10. Maximum Avalanche Energy Vs. Drain Current

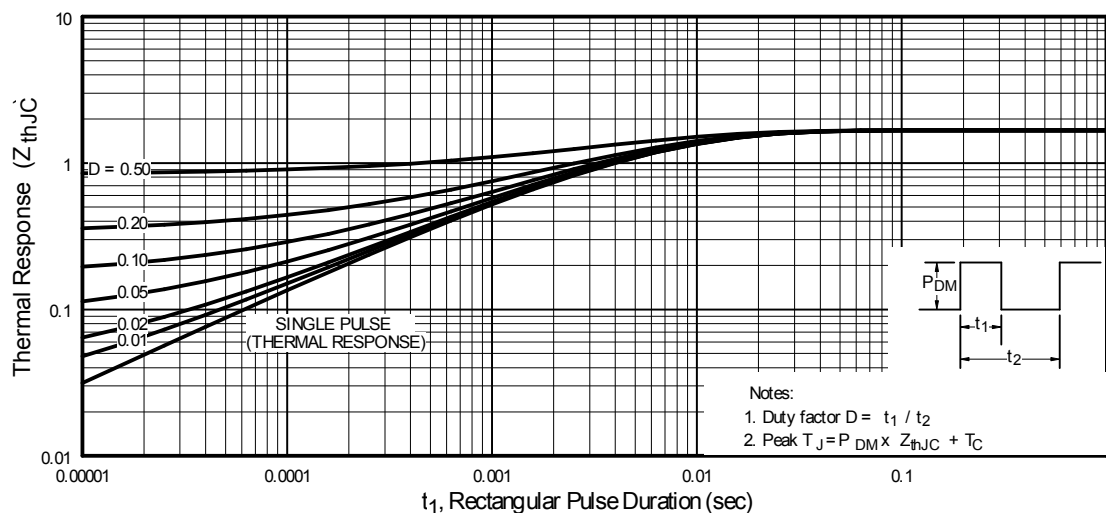


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

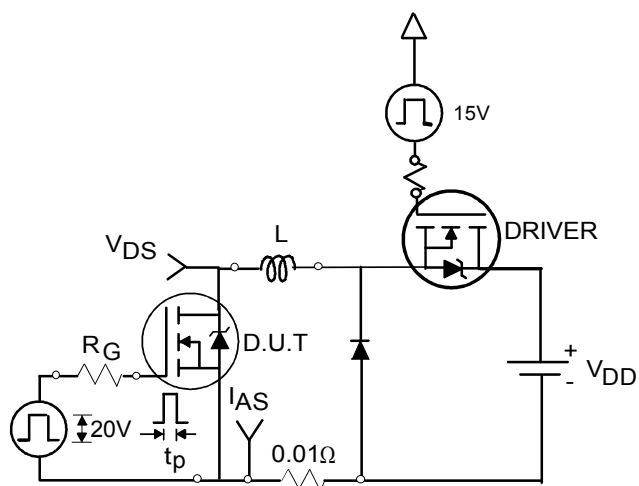


Fig 12a. Unclamped Inductive Test Circuit

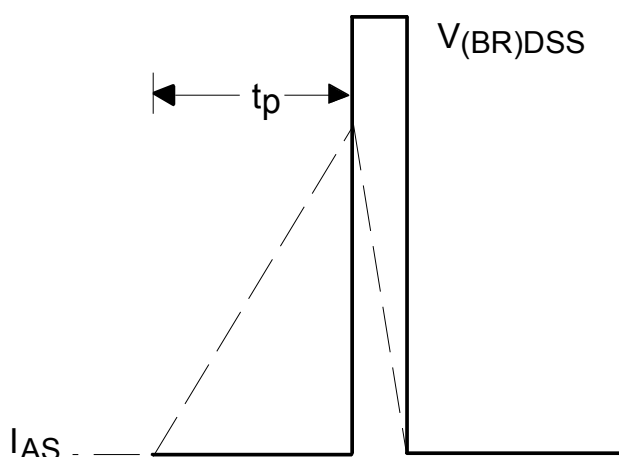


Fig 12b. Unclamped Inductive Waveforms

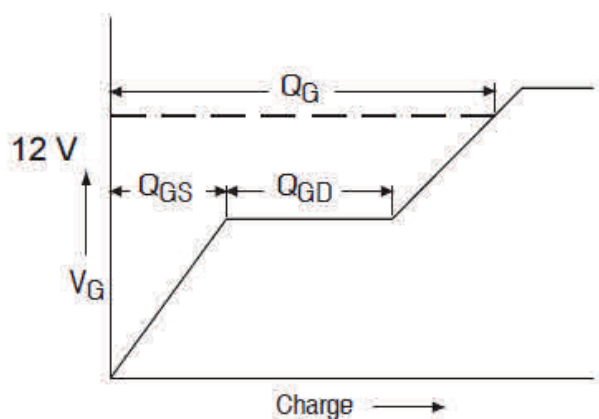


Fig 13a. Gate Charge Waveform

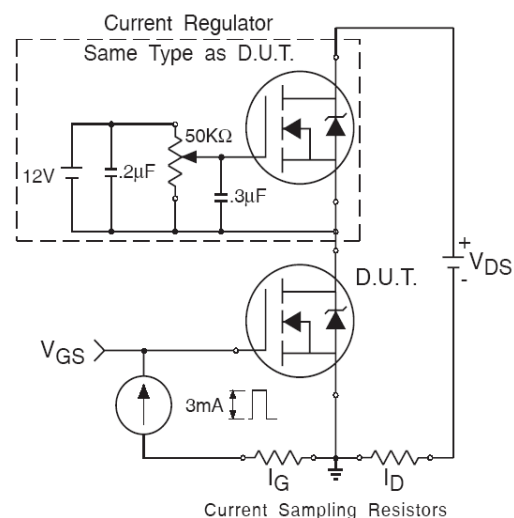


Fig 13b. Gate Charge Test Circuit

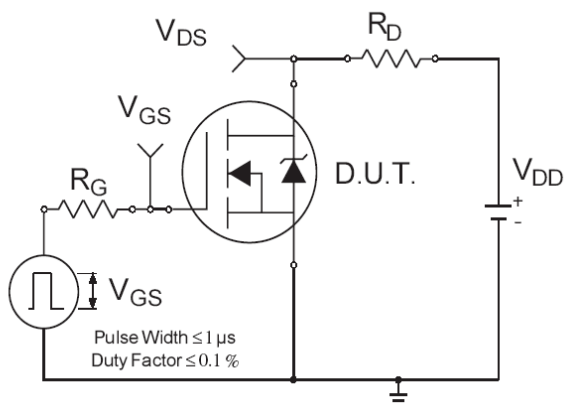


Fig 14a. Switching Time Test Circuit

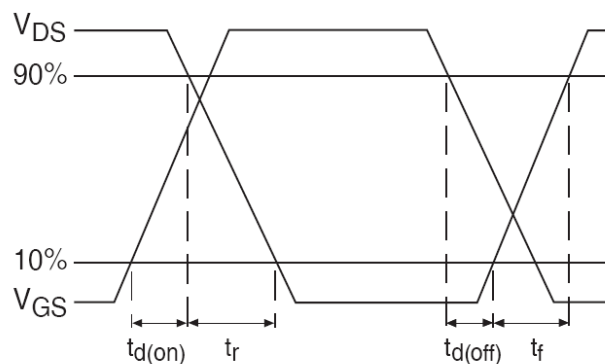
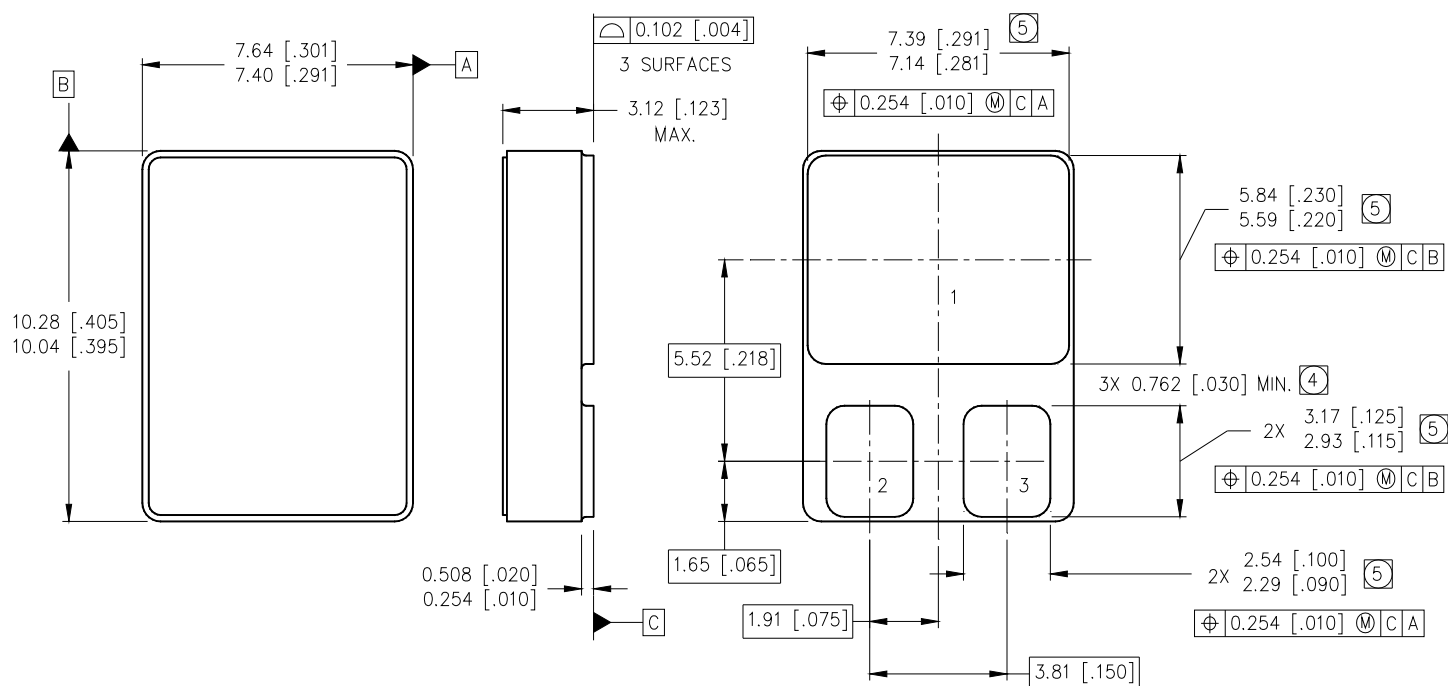


Fig 14b. Switching Time Waveforms

Case Outline and Dimensions — SMD-0.5



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

4
5

DIMENSION INCLUDES METALLIZATION FLASH.

DIMENSION DOES NOT INCLUDE METALLIZATION FLASH.

PAD ASSIGNMENTS

MOSFET

1 = DRAIN

2 = GATE

3 = SOURCE

IMPORTANT NOTICE

The information given in this document shall be in no event regarded as guarantee of conditions or characteristic. The data contained herein is a characterization of the component based on internal standards and is intended to demonstrate and provide guidance for typical part performance. It will require further evaluation, qualification and analysis to determine suitability in the application environment to confirm compliance to your system requirements.

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