32 kHz—100 MHz CMEMS® 振荡器

特性

- 宽带率范围：32 kHz 至 100 MHz
  - 连接 Silicon Labs 于 100 MHz 以上的频率
- Si501 单频，具有 OE
- Si502 双频，具有 OE/FS
- Si503 四频，具有 FS
- ±20/30/50 ppm 频率稳定性包括 10 年老化
- LVCMOS 输出
- 低周期抖动
- 低功耗
- 连续供应电压范围：+1.71 V 至 + 3.63 V
- 可供用户选择的 tRise/tFall 选项
- 无毛刺开始和停止
- 卓越的短期稳定性，长期老化
- 工业标准封装：2x2.5、 2.5x3.2、 3.2x5 mm
- 无铅，符合 RoHS 要求
- 交付周期短：< 2 周
- -20 至 +70 °C: 扩展商用
- -40 至 +85 °C：工业的
- Si50x 系列也包括为接入电路可编程序而设计的 Si504（见 Si504 数据表）

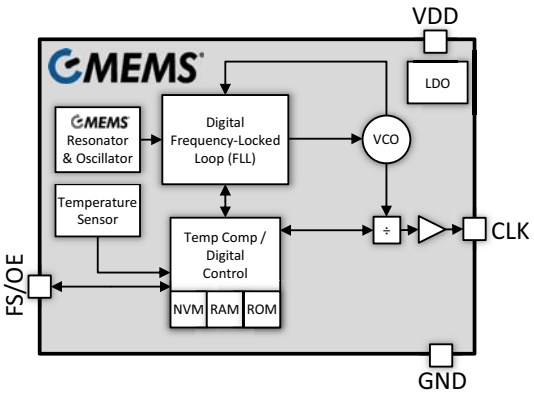
应用

- 存储 (SATA/SAS/PCIe)
- 通用处理器
- 工业控制器
- 嵌入式控制器
- 电动机控制
- 流动控制
- 办公 / 家庭自动化
- IP 摄像机 / 监控
- 显示和控制面板
- 户外电子设备
- 多功能打印机
- 办公设备

描述

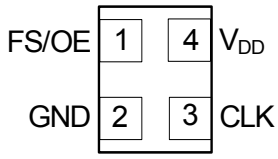
Si501/2/3 CMEMS 振荡器系列提供单片、基于 MEMS 技术的集成电路替代传统的晶体振荡器。Silicon Laboratories 公司的 CMEMS 技术将标准的 CMOS + MEMS 整合于单一的、单片集成电路，从而提供集成的、高品质和高可靠性的振荡器。每个器件都经过出厂测试，并且其配置能够保证性能符合数据表关于电压、工艺、温度、撞击、振动和老化的规格。
其他有关 Si50x CMEMS 振荡器架构和 CMEMS 技术的信息，可浏览 Silicon Labs 公司网站 www.silabs.com/cmems 上的白皮书。

功能框图



订购信息：
详见章节 5。

引脚分配



专利申请中

目录

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1。 电气规格

Table 1. Recommended Operating Conditions

V_{DD}=1.71 to 3.63 V, T_A= –40 to 85 °C, unless otherwise specified

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage[1]	V_{DD}		1.71	—	3.63	V
Supply Current	I_{DD1}	C_L=4 pF, 3.3 V_{DD}, F_{CLK}=1.0 MHz, low power option	—	1.7	2.5	mA
		C_L=4 pF, 3.3 V_{DD}, F_{CLK}=100 MHz, low power option	—	5.3	6.5	mA
		C_L=4 pF, 3.3 V_{DD}, F_{CLK}=1.0 MHz, low jitter option	—	3.9	4.9	mA
		C_L=4 pF, 3.3 V_{DD}, F_{CLK}=100 MHz, low jitter option	—	7.6	8.9	mA
Static Supply Current	I_{DD2}	Mode=Stop[2], low power option F_{CLK}=1 MHz	—	1.7	2.5	mA
		Mode=Stop[2], low jitter option F_{CLK}=1 MHz	—	3.9	4.9	mA
		Mode=Doze[2]	—	670	890	µA
		Mode=Sleep[2]	—	0.3	1	µA
Input High Voltage	V_{IH}	FS/OE pin	0.70 x V_{DD}	—	—	V
Input Low Voltage	V_{IL}	FS/OE pin	—	—	0.30 x V_{DD}	V
OE Internal Pull Resistor	R_I	Ordering option	40	50	60	kΩ
Operating Temperature	T_A	Extended commercial grade	–20	—	70	°C
		Industrial grade	–40	—	85	°C

Notes:

1. The supply voltage range is continuous from 1.71 to 3.63 V.
2. Si501 and Si502 only. Si503 has FS only and does not support Stop, Doze, or Sleep. See Section 3. Functional Description for more information on operational modes.

Table 2. Output Clock Characteristics

V_{DD}=1.71 to 3.63 V, T_A= –40 to 85 °C, unless otherwise specified.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency Range	F_{CLK}		0.032	—	100	MHz
Clock Period	T_{CLK}	$1/F_{CLK}$	31,250	—	10	ns
Total Stability[1]	F_{STAB}		–20	—	+20	ppm
			–30	—	+30	ppm
			–50	—	+50	ppm
Initial Accuracy	F_I	Measured at 25 °C at the time of shipping	—	±2	—	ppm
Startup Time[2]	T_{SU}	From V_{DD} crossing 1.71 V to first clock output	—	2.5	4	ms
Resume Time[3,4]	T_{RUN}	From Sleep mode	—	2.5	5	ms
		From Doze mode	—	1.7	2.55	ms
		From Stop mode[5]	—	—	1.5 x T_{CLK} + 35	ns
Output Disable Time[3,4]	T_D	To Sleep/Doze mode, from output running	—	—	225	µs
		To Stop, from output running	—	—	1.5 x T_{CLK} + 35	ns
Frequency Update Time[4,6]	T_{NEW_FREQ}		—	—	5	ms

Notes:

1. Orderable option. Stability budget consists of initial tolerance, operating temperature range, rated power supply voltage change, load change, 10-year aging, shock, and vibration.
2. Hold FS/OE high (strong or weak) during powerup for fastest time to clock.
3. Si501 and Si502 only. Si503 has FS only and does not support Stop, Doze, or Sleep.
4. Asserted FS/OE actions must be held stable for the maximum duration of the invoked FS/OE event (e.g., T_{RUN}, T_{NEW_FREQ}, T_D, etc).
5. If the Si502 frequency is switched while the device is in Stop mode, the frequency prior to Stop will be output briefly until the glitchless switch to the other frequency. Doze mode and Sleep mode do not have this behavior.
6. Si502 and Si503 only. Si501 is a single frequency device with OE only.

Table 3. Output Clock Levels and Symmetry

V_{DD} = 1.71 to 3.63 V, T_A = –40 to 85 °C unless otherwise indicated.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage	V_{OH}	1st ordering option code: A and H I_{OH}=–4 mA	0.90 x V_{DD}	—	—	V
Output Low Voltage	V_{OL}	1st ordering option code: A and H I_{OH}=+4 mA	—	—	0.10 x V_{DD}	V
Rise/Fall Time[1]	tRise /tFall	1st ordering option code[2]: A and H Z_0=25 Ω @ 3.3 V	0.4	0.7[2]	1.2	ns
		1st ordering option code: B and J Z_0= 50 Ω @ 3.3 V	1	1.3	1.6	ns
		1st ordering option code: C and K Z_0= 50 Ω @ 2.5 V	1	1.3	1.6	ns
		1st ordering option code: D and L Z_0 = 50 Ω @ 1.8 V	1	1.3	1.6	ns
		1st ordering option code: E and M Z_0= 110 Ω @ 3.3 V	2	3	4	ns
		1st ordering option code: F and N Z_0=220 Ω @ 3.3 V	4	5	7	ns
		1st ordering option code: G and P Z_0=440 Ω @ 3.3 V	7	8	11	ns
Duty Cycle	DC	Drive strength selected such that tRise/tFall (20% to 80%)<10% of period	45	50	55	%

Notes:
1. C_L=15 pF, tRise/tFall (20% to 80%), 3.3 V, unless otherwise stated.
2. Recommended series termination resistor (R_S) = 24.9 Ω for Z_0=50 Ω.

Table 4. Output Clock Jitter and Phase Noise

V_{DD} = 1.71 to 3.63 V, T_A = –40 to 85 °C unless otherwise indicated.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Cycle-to-Cycle Jitter	J_{CCPP}	100 MHz, Low Jitter Option 1st ordering option code: H	—	14	25	ps pk-pk
		100 MHz, Low Power Option 1st ordering option code: A	—	16	26	ps pk-pk
Period Jitter	J_{PRMS}	100 MHz, Low Jitter Option 1st ordering option code: H	—	1	1.6	ps rms
		100 MHz, Low Power Option 1st ordering option code: A	—	1.3	1.9	ps rms
Period Jitter Pk-Pk	J_{PPKPK}	Low Jitter Option 10k samples 1st ordering option code: H	—	9	13	ps pk-pk
		Low Power Option 10k samples 1st ordering option code: A	—	10	16	ps pk-pk
Phase Jitter[1]	ϕ	75 MHz F_{OFFSET}=900 kHz to 7.5 MHz Low Jitter Option 1st ordering option code: H	—	1	1.3	ps rms
		75 MHz F_{OFFSET}=900 kHz to 7.5 MHz Low Power Option 1st ordering option code: A	—	2.5	3.2	ps rms

Notes:

1. Integrated phase jitter exceeds the requirements of some high-performance data communications systems. See AN783 for additional information.

Table 5. Environmental Compliance and Package Information

Parameter	Test Condition
Mechanical Shock	MIL-STD-883, Method 2002, Cond B. (1,500 g)
Mechanical Shock High g	MIL-STD-883, Method 2002, Cond E. (10,000 g)
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Temperature Cycle	JESD22, Method A104
Resistance to Solder Heat	MIL-STD-883, Method 2036
Contact Pads	Gold over Nickel/Palladium

Table 6. Thermal Conditions

Parameter	Symbol	Test Condition	Value	Unit
Thermal Impedance	θ_{JA}	3.2x5 mm, still air	187	°C/W
		2.5x3.2 mm, still air	239	
		2x2.5 mm, still air	241	

Table 7. Absolute Maximum Limits[1]

Parameter	Symbol	Rating	Unit
Maximum Operating Temperature	T_{MAX}	85	°C
Storage Temperature	T_S	–55 to +125	°C
Supply Voltage	V_{DD}	–0.5 to +3.8	V
Input Voltage	V_{IN}	–0.5 to V_{DD} +0.3V	V
ESD Sensitivity (JESD22-A114)	HBM	2000	V
ESD Sensitivity (CDM)	CDM	500	V
Soldering Temperature (Pb-free profile)[2]	T_{PEAK}	260	°C
Soldering Time at T_{PEAK} (PB-free profile)[2]	T_P	20–40	s
Junction Temperature	T_J	125	°C

Notes:
1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020.

2。 Si501/2/3 典型应用电路、交流波型和功能说明

根据所选器件及订购配置选项，Si501/2/3 系列具有各种应用电路和交流波型。阅读下面部分时请特别注意，确定您参考的是正确的图表。

2.1。 Si501/2 应用电路

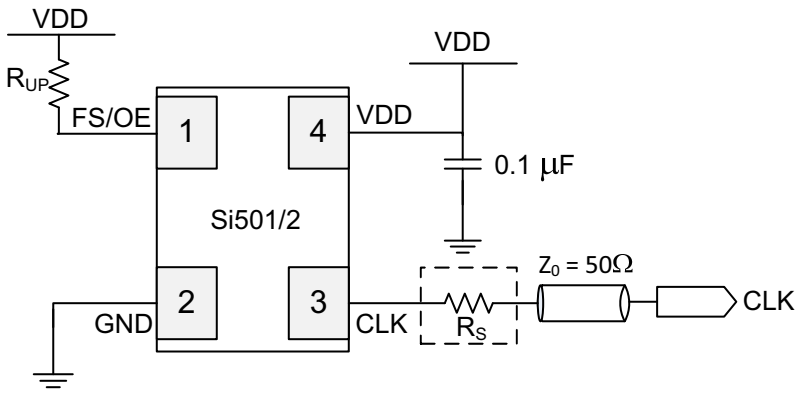
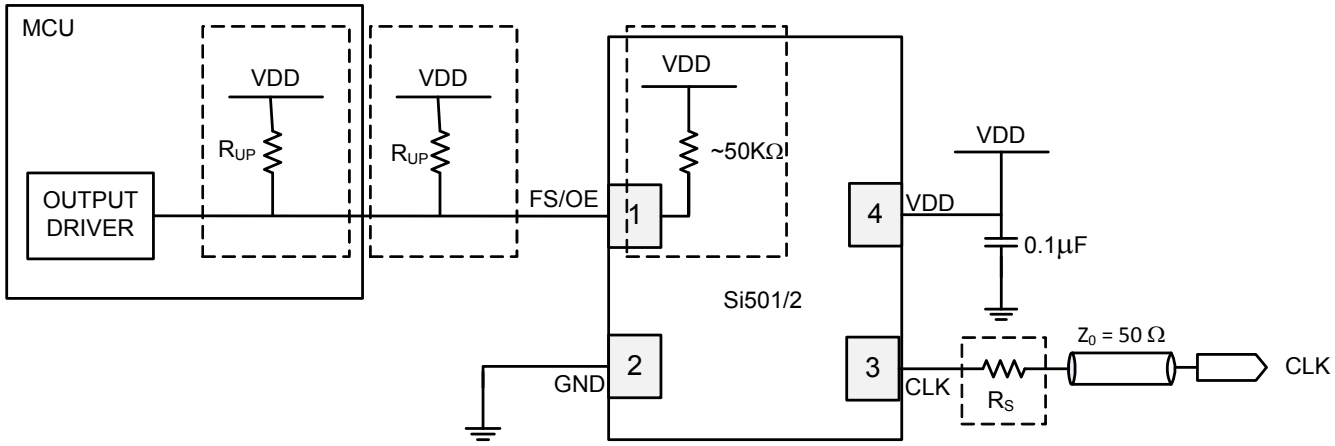


Figure 1. Si501/2 Applications Circuit with Optional Output Series Resistor

注意： 在图 1 中的虚线框代表取决于 tRise/tFall 的配置选项的一个可选部件。该图表适用于所有的 Si50x 产品驱动强度配置选项。见 Table 3 中的 R_S 推荐。配置选项请见第 5。 “ 订购指南 ” 节。



注意： 图 2 的虚线框表明电阻器选项取决于 MCU 上拉电阻器配置和 Si501/2 内部电阻器配置选项。配置选项请见第 5。 “ 订购指南” 节。用户只能设计引脚 1 虚线框选项中的一个。引脚 3 的串联电阻器 (R_S) 也是可选择项。见Table 3 中的 R_S 推荐。

Figure 2. Si501/2 Applications Circuit with MCU Configuration Options

Table 8. Si502 FS/OE States and Resistor Values

FS/OE Pin State	R_{UP}	Clock Output
Strong High	$0\ \Omega \le R_{UP} \le 1\ k\Omega$	Frequency 1
Weak High	$20\ k\Omega \le R_{UP} \le 200\ k\Omega$	Frequency 2
Low	—	Hi-Z

Notes:
1. If the Si502 internal pull-up resistor configuration option is not selected, an MCU internal pull-up resistor or an external pull-up resistor should be used.
2. The parallel combination of all pull-up resistors on the FS/OE pin, including the optional internal device pull-up resistor must be > 20 kΩ to select the Weak High state.
3. If the Si502 internal pull-up resistor is enabled with no other external FS/OE connections, the FS/OE state will be detected as `Weak High' which selects the Frequency 2 output by default.

2.2。 Si501/2 交流波形和功能说明

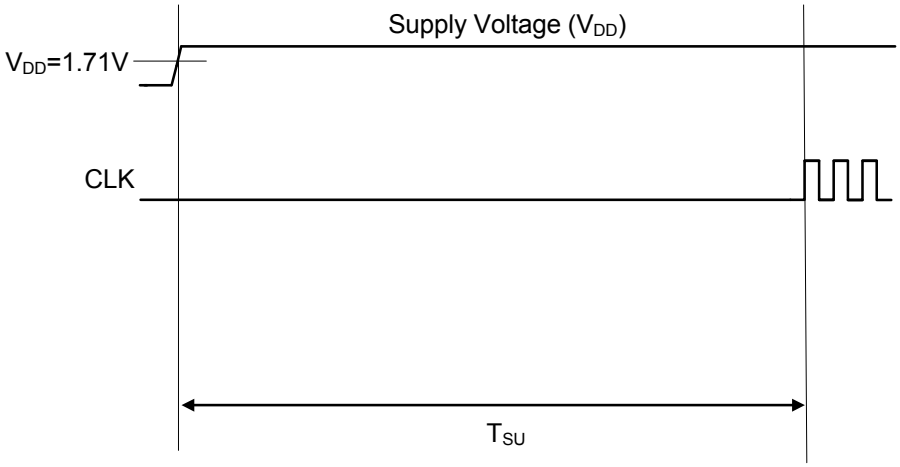


Figure 3. Si501/2 Power On Time (refer to Table 2)

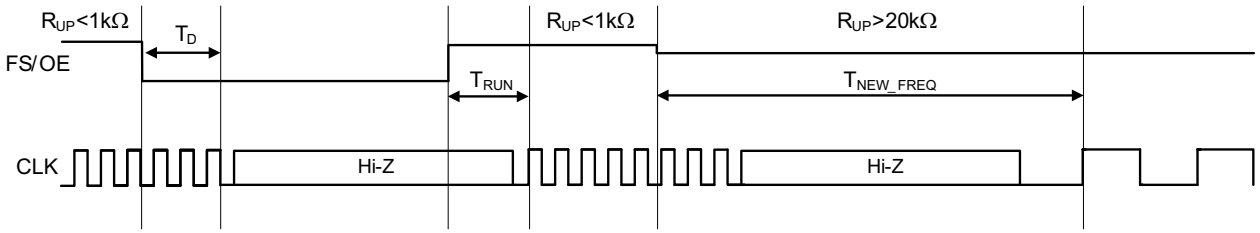
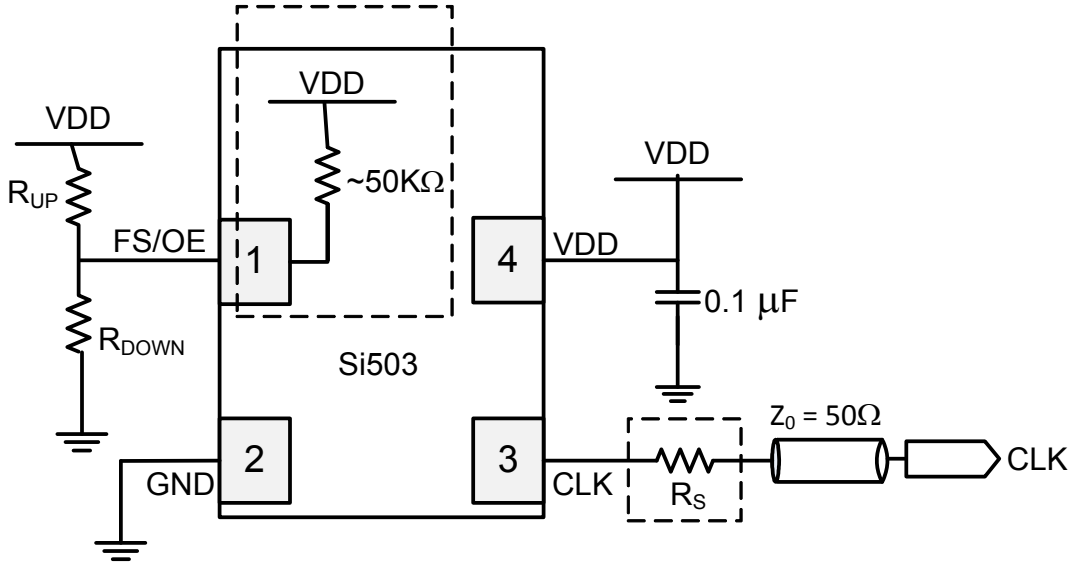


Figure 4. Si501/2 AC Waveform (refer to Table 2)

2.3。 Si503 应用电路

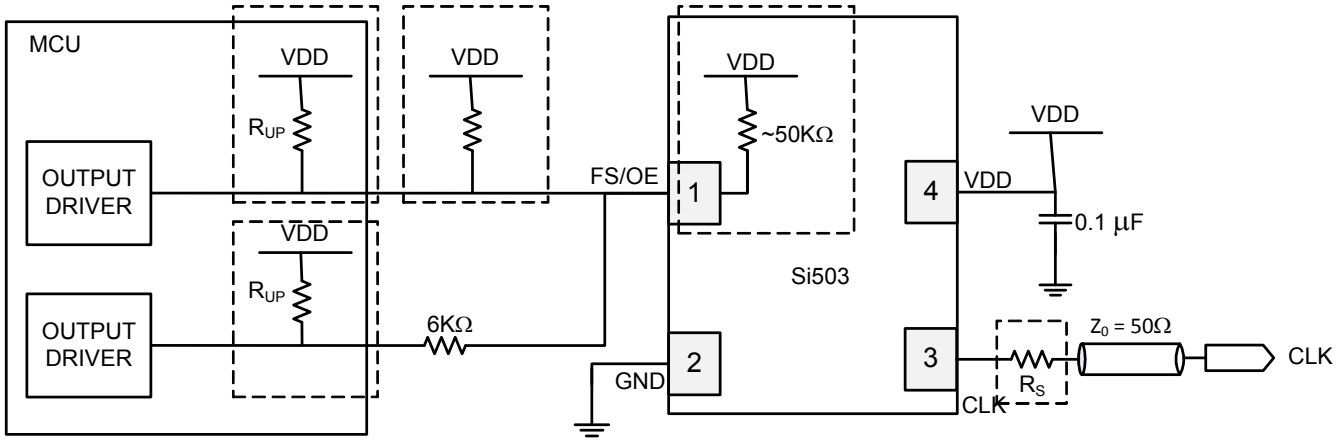


注意： 虚线框表明可选择的部件取决于 tRise/tFall 和内上拉电阻器配置选项。配置选项请见第 5。 “ 订购指南 ” 节。见 Table 3 中的 R_S 推荐。

Figure 5. Si503 Applications Circuit with Configuration Options

Table 9. Si503 Frequency Select with External Resistor Options

FS/OE Pin State	R_{UP}	R_{DOWN}	Clock Output
Strong High	$0\ \Omega \le R_{UP} \le 1\ k\Omega$	Do not populate	Frequency 1
Weak High	$20\ k\Omega \le R_{UP} \le 200\ k\Omega$	Do not populate	Frequency 2
Weak Low	Do not populate	$20\ k\Omega \le R_{DOWN} \le 200\ k\Omega$	Frequency 3
Strong Low	Do not populate	$0\ \Omega \le R_{DOWN} \le 1\ k\Omega$	Frequency 4
Note: If the Si503 internal pull-up resistor is enabled with no other external FS/OE connections, the FS/OE state will be detected as `Weak High' which selects the Frequency 2 output by default.			



注意： 图 6 的虚线框表明电阻器选项取决于 MCU 上拉电阻器配置和 Si503 内部电阻器配置选项。配置选项请见第 5。“订购指南”节。用户只能设计引脚 1 虚线框选项中的一个。引脚 3 的串联电阻器（R_S）也是可选择项。见Table 3 中的 R_S 推荐。

Figure 6. Si503 Applications Circuit with MCU and Configuration Options

Table 10. Si503 Frequency Select

FS/OE Pin State	MCU Output 1	MCU Output 2	Clock Output
Strong High	High	Hi-Z	Frequency 1
Weak High	Hi-Z	Hi-Z	Frequency 2
Weak Low	Hi-Z	Low	Frequency 3
Strong Low	Low	Hi-Z	Frequency 4
Note: If the Si50x internal pull-up resistor is enabled with no other external OE connections, the OE state will be detected as `Weak High' which selects the Frequency 2 output by default.			

2.4。 Si503 交流波型和功能说明

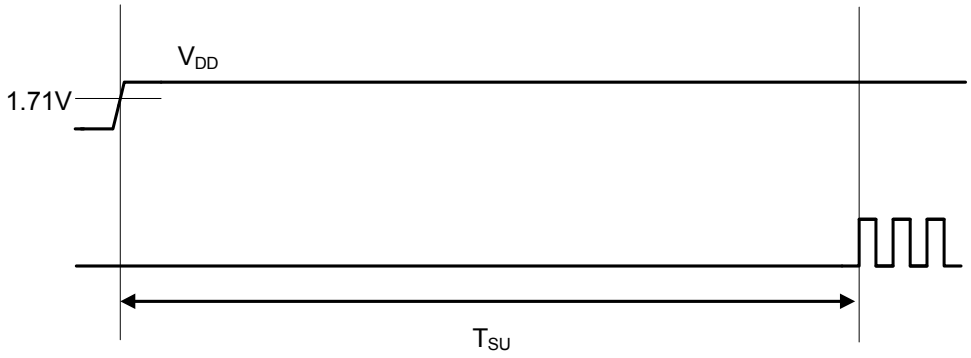


Figure 7. Si503 Power On Time (refer to Table 2)

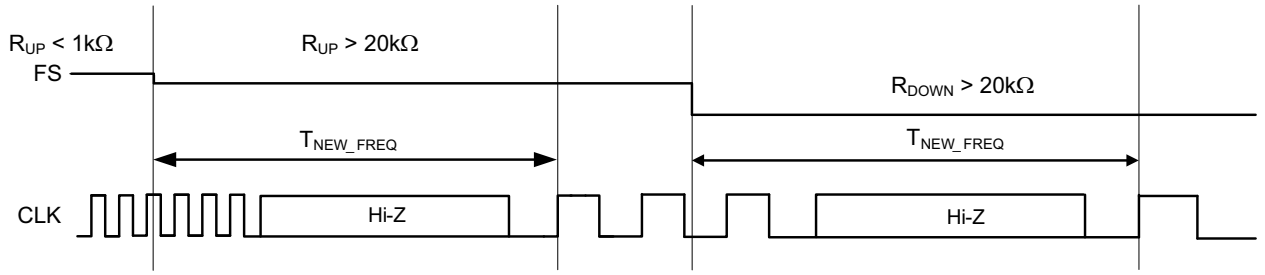


Figure 8. Si503 AC Waveform (refer to Table 2)

3。 功能描述

Si50x 系列的振荡器系列包含四种基本器件。所有器件都可根据第 5。 “ 订购指南 ” 节进行配置。四种器件中的每一种在任意时间均可支持单一时钟输出频率，并根据它们在片上内存上存储的时钟频率数量分段。

Si501 支持单一存储频率，通过 OE 功能启用。 Si502 存储两个频率，可通过 FS 选择并通过 OE 功能启用或禁用。 Si503 存储四个频率，通过 FS 功能选择。 Si503 不支持 OE 功能。本数据表将对 Si501/2/3 进行说明。

Si504 是一款可编程振荡器，通过一个单引脚接口（C1D）进行控制。这部分内容请见 www.siliconlabs.com/cmems 上相应的 Si504 数据表。

Si50x CMEMS 系列中的所有器件均采用成本优化、低功耗数字的 FLL 架构，以通过被动补偿 MEMS 谐振器参考频率生成高度准确且稳定的输出时钟。

此架构使用 MEMS 谐振器作为参考时钟，并使用芯片上的分频信号和数控 VCO 驱动 FLL 数字环路滤波器的频率比较器。数字环路滤波器累积并进一步处理频率误差值以生成目标输出频率。

该架构还使用高分辨率、低噪音温度传感器和温度补偿算法以抵消被动补偿 MEMS 谐振器的任何温度漂移。每种器件都经过温度校准，然后 MEMS 谐振器频率配对并衍生出一个器件特定的补偿多项式。随着温度发生变化，此补偿电路会补偿所有频率漂移。

因为 MEMS 谐振器和 CMOS 补偿电路在一个单块芯片中，并因此有几个微米的间隔，所以这个紧密耦合的系统极其准确、快速。

整个系统处理在一秒内发生数千次，温度变化时 （包括任何快速的温度瞬变）可提供极佳的频率准确性和稳定性。此振荡器还支持低功耗版本，它将采样周期降低到一个较长的周期，这为放松抖动规格约为 1 ps RMS 的应用减少了约为 2-3 mA 的功耗。具体规格请参见 Table 1。

3.1。 OE 启用和禁用状态

Si50x CMEMS 系列通过 FS/OE 配置引脚支持四种操作输出状态。启用后， Si50x 处于运行模式，时钟为输出，功耗如Table 1 中所示。禁用模式为 “停止” 、 “睡眠” 和 “休眠” 。每种状态的功耗都不尽相同，如Table 1 中所示。

3.1.1。停止模式

停止模式下的 Si50x 输出为高阻抗，又称高阻 (Hi-Z) 或三态。停止模式禁用输出驱动，但数字核心和 MEMS 谐振器仍然保持启用，从而能够快速转换到 “ 运行 ” 模式。无故障完成最后一个循环后，输出停止并保持在高阻状态。 “ 停止 ” 模式下不采取任何其他节能措施。

3.1.2。休眠模式

休眠模式下的 Si50x 输出为高阻抗，又称高阻 (Hi-Z) 或三态。休眠模式禁用输出驱动、 VCO 和 MEMS 谐振器，但数字核心仍然保持启用。无故障完成最后一个循环后，输出停止并保持在并保持在高阻状态。

3.1.3。睡眠模式

睡眠模式下的 Si50x 输出为高阻抗，又称高阻 (Hi-Z) 或三态。除保留最后一次器件配置的低泄漏电路外，睡眠模式禁用所有电路的电源。无故障完成最后一个循环后，输出停止并保持在并保持在高阻状态。

3.2。 输出上升和下降设置

Si50x 时钟输出是可编程的。这样可降低时钟输出的电磁干扰 （EMI）辐射。 EMI 的降低数量取决于输出频率、目标谐波和电路板设计。实验室结果使用 50 MHz FOUT 并将时钟 tRise/tFall 时间从 0.7 ns 改为 8 ns，显示最高有 14 dB 的 EMI 降低。

tRise/tFall 功能还使 Si50x 能够匹配竞争器件的上升和下降时间。晶体振荡器的 tRise/tFall 行为很大程度上取决于电源电压。在基于晶体的振荡器中，更高的电源电压通常会造成更急促的 tRise/tFall 时间。Si50x 配置选项使用户能够将 tRise/tFall 与电源电压匹配。通过给定的电源电压和 50 Ω 的走线阻抗，Si50x 还可提供指定的 tRise/tFall。Si50x tRise/tFall 规格请见 Table 3。

4。 引脚描述

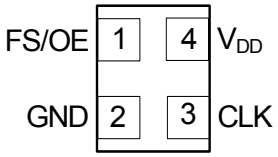


Figure 9. Si501/2/3

Table 11. Pin Description

Pin	Name	Function
1	FS/OE	FS=Frequency Select. Si502 and Si503 only. OE=Output Enable. Si501 and Si502 only.
2	GND	Ground.
3	CLK	Output clock.
4	V_{DD}	Power supply. Bypass with a 0.1μF capacitor placed as close to the V_{DD} pin as possible.

5。 订购指南

CMEMS 的振荡器 Si50x 系列具有高度的可配置性。根据下面的指导方针，为每一个可订购的零件设定编号。保证每个定制零件的性能均可在符合数据表规格的条件下运行。在线配置和订购工具请见 www.siliconlabs.com/cmems。

5.1。 Si501 订购指南和零件编号语法

	VDD	Jitter vs Power	TYP T_R/T_F
A	1.7-3.6	Low Power	0.7 ns[1]
B	3.3V		1.3 ns[2]
C	2.5V		1.3 ns[2]
D	1.8V		1.3 ns[2]
E	1.7-3.6		3 ns[3]
F	1.7-3.6		5 ns[3]
G	1.7-3.6		8 ns[3]
H	1.7-3.6	Low Jitter	0.7 ns[1]
J	3.3V		1.3 ns[2]
K	2.5V		1.3 ns[2]
L	1.8V		1.3 ns[2]
M	1.7-3.6		3 ns[3]
N	1.7-3.6		5 ns[3]
P	1.7-3.6		8 ns[3]

	OE High	OE Low	Internal Pull Resistor
A	Enable	Stop	Pull-Up
B	Enable	Doze	Pull-Up
C	Enable	Sleep	Pull-Up
D	Stop	Enable	Pull-Down
E	Doze	Enable	Pull-Down
F	Sleep	Enable	Pull-Down
G	Enable	Stop	None
H	Enable	Doze	None
J	Enable	Sleep	None
K	Stop	Enable	None
L	Doze	Enable	None
M	Sleep	Enable	None

	Package Dimension
B	3.2 x 5 mm[4]
C	2.5 x 3.2 mm
D	2 x 2.5 mm

	Temp Range
F	-20 to 70 °C
G	-40 to 85 °C

	Reel
R	Reel
	Cut Tape

501 J C A - - - - - - - D A G R

Revision

OPN Prefix	Description
501	Single frequency
502	Dual frequency
503	Quad frequency
504	Any frequency

	Ppm
A	± 50
B	± 30
C	± 20

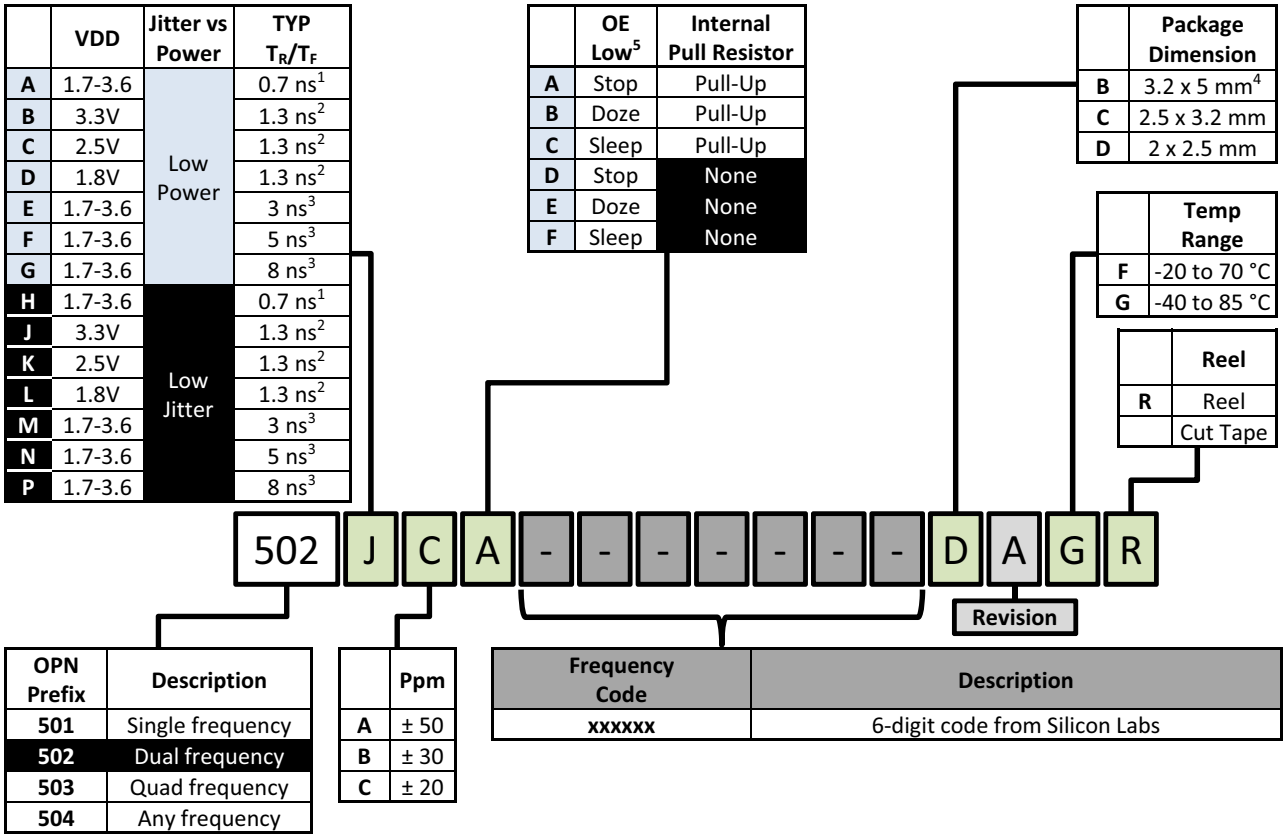
Frequency Code	Description
Mxxxxxx	f_{OUT} < 1 MHz
xMxxxxx	1 MHz ≤ f_{OUT} < 10 MHz
xxMxxxx	10 MHz ≤ f_{OUT} < 100 MHz
100M000	f_{OUT} = 100 MHz
xxxxxx	6-digit code for > 6 decimal resolution

Notes:

1. Series termination resistor (R_S) is recommended for this configuration. SeeTable 3 and Section 2.
2. Series termination resistor is not needed for this configuration. Output impedance is 50 Ω for the indicated supply condition.
3. Series termination resistor is not needed for this configuration. Reduced EMI setting.
4. Silicon Labs 3.2 x 5 mm package is delivered as 3.2 x 4 mm and accommodates the industry-standard 3.2 x 5 mm footprint.

Figure 10. Si501 Part Number Syntax

5.2。 Si502 订购指南和零件编号语法

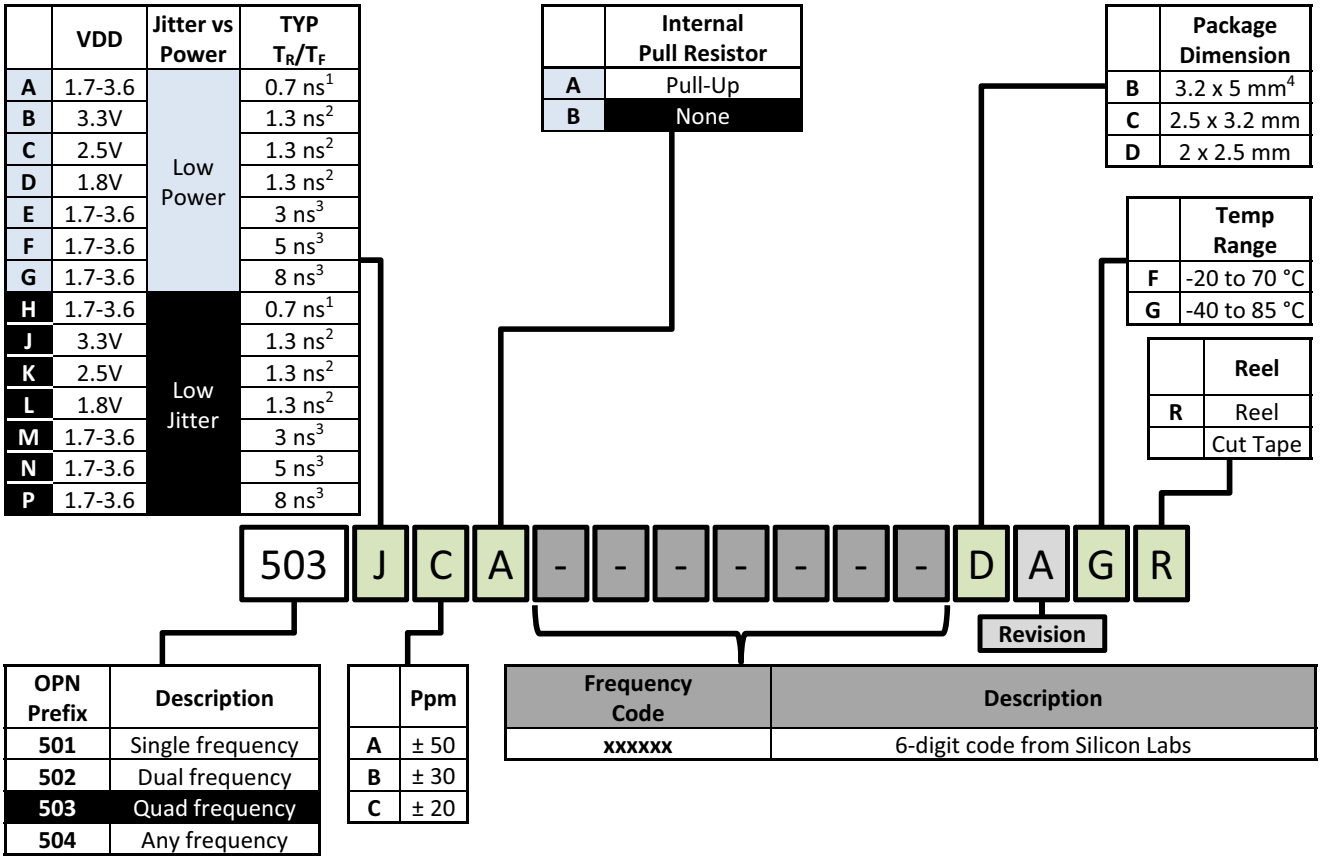


Notes:

1. Series termination resistor (R_S) is recommended for this configuration. See Table 3 and Section 2.
2. Series termination resistor is not needed for this configuration. Output impedance is 50 Ω for the indicated supply condition.
3. Series termination resistor is not needed for this configuration. Reduced EMI setting.
4. Silicon Labs 3.2 x 5 mm package is delivered as 3.2 x 4 mm and accommodates the industry-standard 3.2 x 5 mm footprint.
5. The Si502 OE pin has three (3) states: OE High = Freq 1; OE Weak High = Freq 2; OE Low is configurable.

Figure 11. Si502 Part Number Syntax

5.3。 Si503 订购指南和零件编号语法



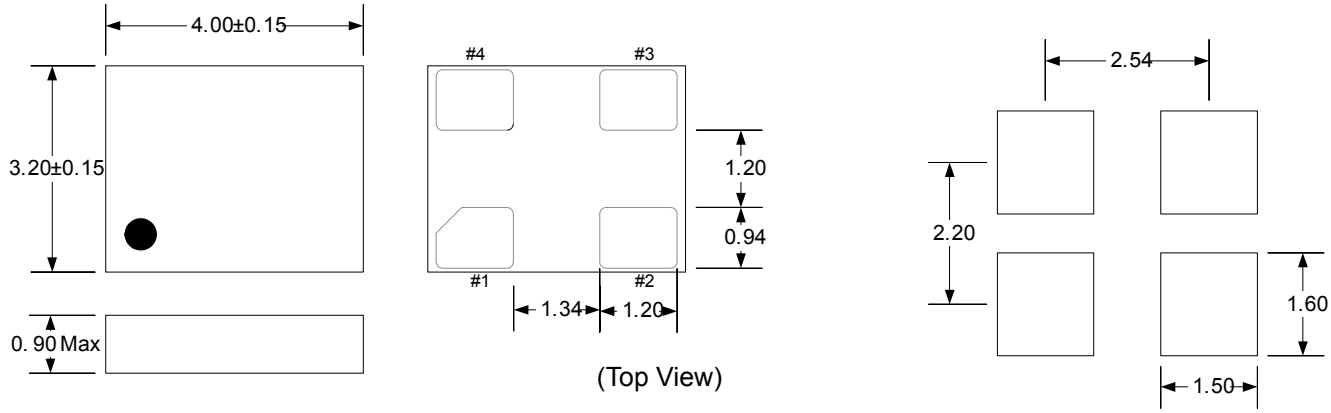
Notes:

1. Series termination resistor (R_S) is recommended for this configuration. See Table 3 and Section 2.
2. Series termination resistor is not needed for this configuration. Output impedance is 50 Ω for the indicated supply condition.
3. Series termination resistor is not needed for this configuration. Reduced EMI setting.
4. Silicon Labs 3.2 x 5 mm package is delivered as 3.2 x 4 mm and accommodates the industry-standard 3.2 x 5 mm footprint.

Figure 12. Si503 Part Number Syntax

6。 封装尺寸和连接盘图形

6.1。 封装外形：3.2×5mm 4 引脚 DFN



Note: The 3.2 x 5 mm package is delivered as a 3.2 x 4 mm package and is drop-in compatible to industry-standard 3.2 x 5 landing patterns.

Figure 13. 3.2 x 5 mm 4-pin DFN

6.2。 封装外形：2.5×3.2mm 4 引脚 DFN

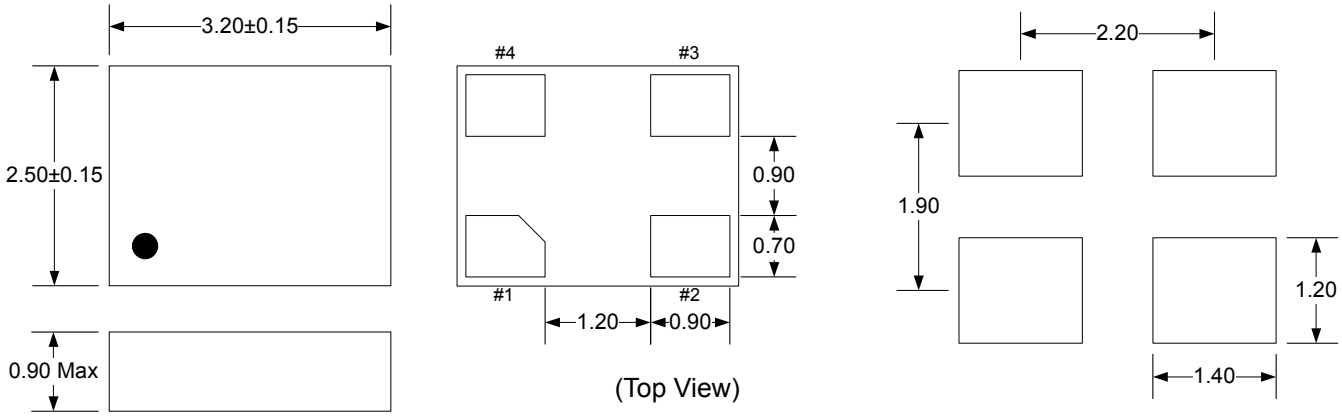


Figure 14. 2.5 x 3.2 mm 4-pin DFN

6.3。 封装外形：2×2.5mm 4 引脚 DFN

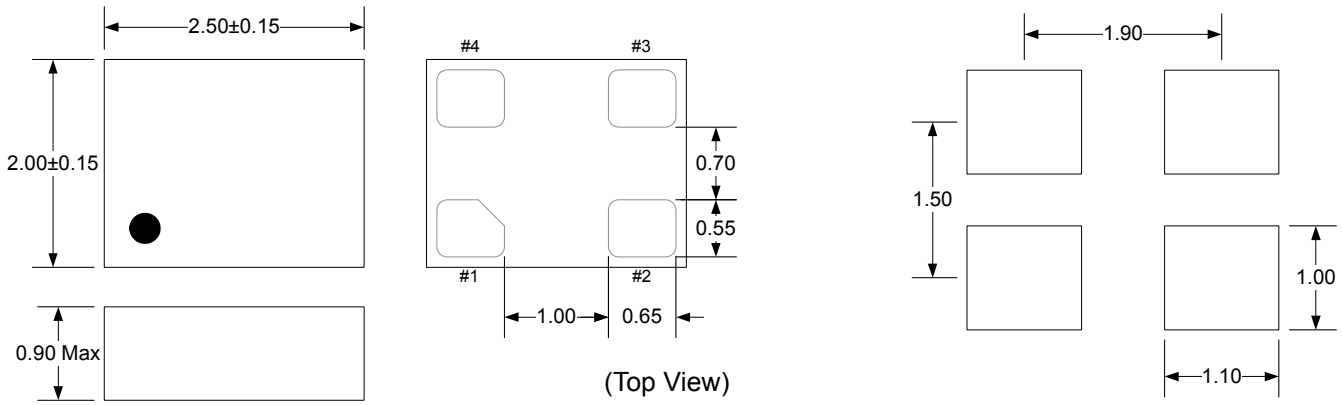
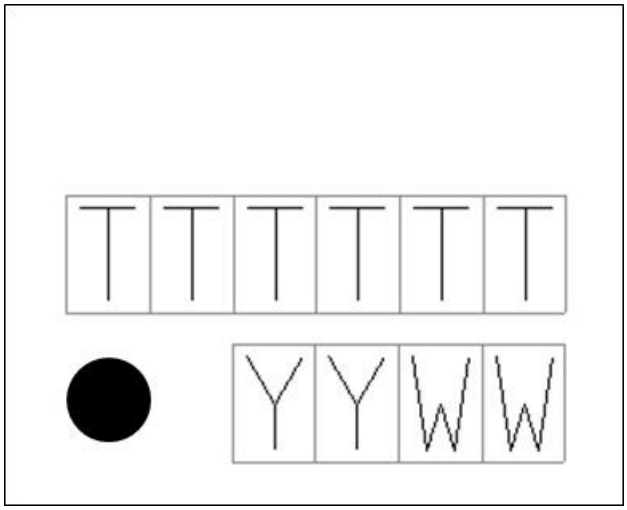


Figure 15. 2 x 2.5 mm 4-pin DFN

7。 顶部标记

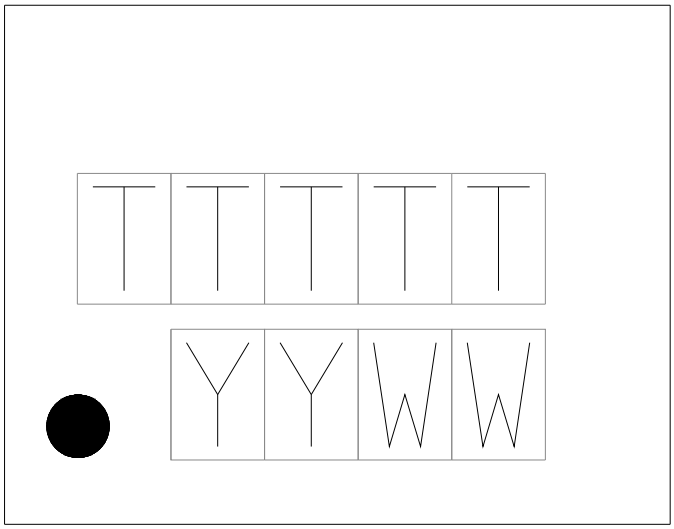
7.1。 3.2×5mm 顶标



7.2。 3.2×5mm 顶标说明

Mark Method:	Laser	
Font Size:	0.60 mm Right-Justified	
Line 1 Marking:	TTTTTT=Trace Code	Manufacturing Code from the Assembly Purchase Order form.
Line 2 Marking	Circle=0.5 mm Diameter Left-Justified	Pin 1 Indicator
	YY=Year WW=Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the build date.

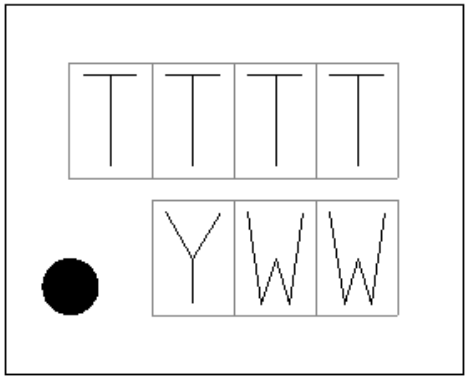
7.3。 2.5×3.2mm 顶标



7.4。 2.5×3.2mm 顶标说明

Mark Method:	Laser	
Font Size:	0.50 mm Right-Justified	
Line 1 Marking:	TTTTT=Trace Code	Manufacturing Code from the Assembly Purchase Order form.
Line 2 Marking:	Circle=0.3 mm Diameter Left-Justified	Pin 1 Indicator
	Y=Year WW=Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the build date.

7.5。 2×2.5mm 顶标



7.6。 2×2.5mm 顶标说明

Mark Method:	Laser	
Font Size:	0.50 mm Right-Justified	
Line 1 Marking:	TTTT=Trace Code	Manufacturing Code from the Assembly Purchase Order form.
Line 2 Marking:	Circle=0.3 mm Diameter Left-Justified	Pin 1 Indicator
	Y=Year WW=Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the build date.

文档更改列表

修订版 0.2 至修订版 0.3

- 合并了 Si501/2/3 数据表。
- 修改了扉页。
- 修改了表 2。
- 修改了表 4。
- 修改了第 2 节。
- 修改了第 3 节。
- 修改了第 4 节。
- 修改了第 5 节。

修订版 0.3 至修订版 0.4

- 修改了扉页。
- 修改了表 1。
- 修改了表 2。
- 修改了表 3。
- 修改了表 4。
- 修改了表 5。
- 修改了表 6。
- 修改了表 7。
- 修改了第 2 节。
- 修改了第 4 节。
- 修改了第 5 节。
- 修改了第 6 节。

修订版 0.4 至修订版 0.41

- 修改了表 4。

修订版 0.41 至修订版 0.7

- 修订后的支持频率范围。
- 在所有相关表中添加最小 / 最大数字。

修订版 0.7 至修订版 0.71

- 修订了表 3。
- 修订了第 5 节。

修订版 0.71 至修订版 0.72

- 修订了表 1。
- 修订了表 2。
- 修订了表 3。
- 修订了表 5。
- 修改了第 2 节。
- 增加了第 3 节。
- 修改了第 4 节。

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