RAA230409 Evaluation Board

R19UH0097EU0000_RAA23040
Rev.1
9/11/2013

3-ch Step-Down Switching Regulator + 1-ch LDO

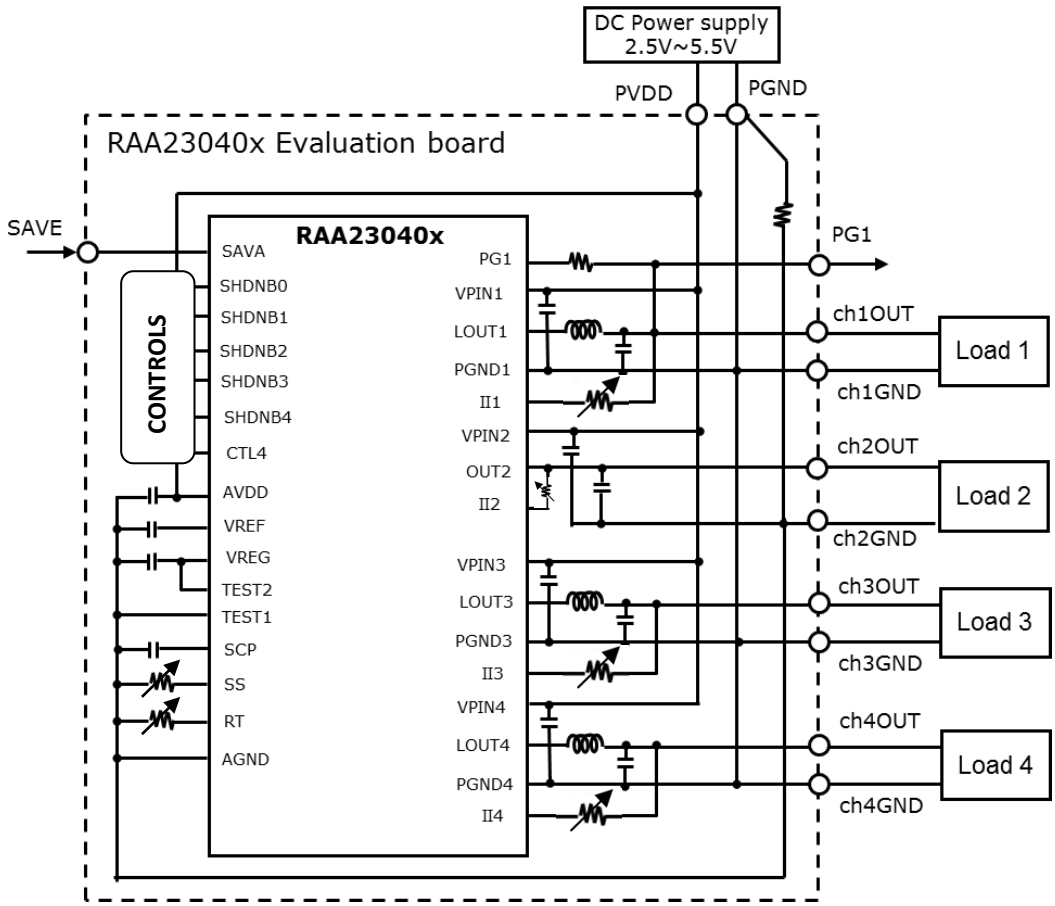
Introduction

The RAA23040x is a monolithic power supply IC that has 3 step-down Switching Regulators with integrated power MOSFETs and one LDO. This application note contains support documentation for the RAA230409 evaluation board including the schematic, the layout and the bill of materials for the board. Also, please refer to the RAA23040x datasheet for more details on the device.

Bard specification

- Input voltage range : 2.5V~5.5V
- Board : 4 layers / FR-4 / components mounted on only one side
- Size (W x D) : 80mm x80mm

Board block diagram and example of connection



Outline of RAA23040x Specification

Configuration

ch	Type	Input Voltage Range	Output Voltage Range	Output Current (MAX)	Switching Frequency
1	Switching * (step-down)	2.5V to 5.5V	0.9V to VIN×0.8	500mA	1.3 MHz to 2 MHz (variable)
2	LDO			100mA	
3	Switching * (step-down)			1500mA	
4	Switching * (step-down)			1500mA	

Note: * Synchronous rectification and Current mode type

Product Lineup Table

The following 9 products are developed based on output voltage.

ch	RAA230401	RAA230402	RAA230403	RAA230404	RAA230405	RAA230406	RAA230407	RAA230408	RAA230409
1	1.8 V	2.5 V	3.0 V	3.3 V	1.8 V	2.5 V	3.0 V	3.3 V	Adjustable
2									
3	3.3 V				Adjustable				
4	Output voltage is selectable. 1.2 V preset voltage by internal resistor or adjustable by external resistor.								

Note: ch1, ch2: RAA230401 to RAA230408 output preset voltage by internal resistor. RAA230409 outputs adjustable voltage by external resistor.

ch3: RAA230401 to RAA230404 output preset voltage by internal resistor. RAA230405 to RAA230409 output adjustable voltage by external resistor.

ch4: All products have switchable output voltage between 1.2 V preset voltage by internal resistor and adjustable voltage by external resistor.

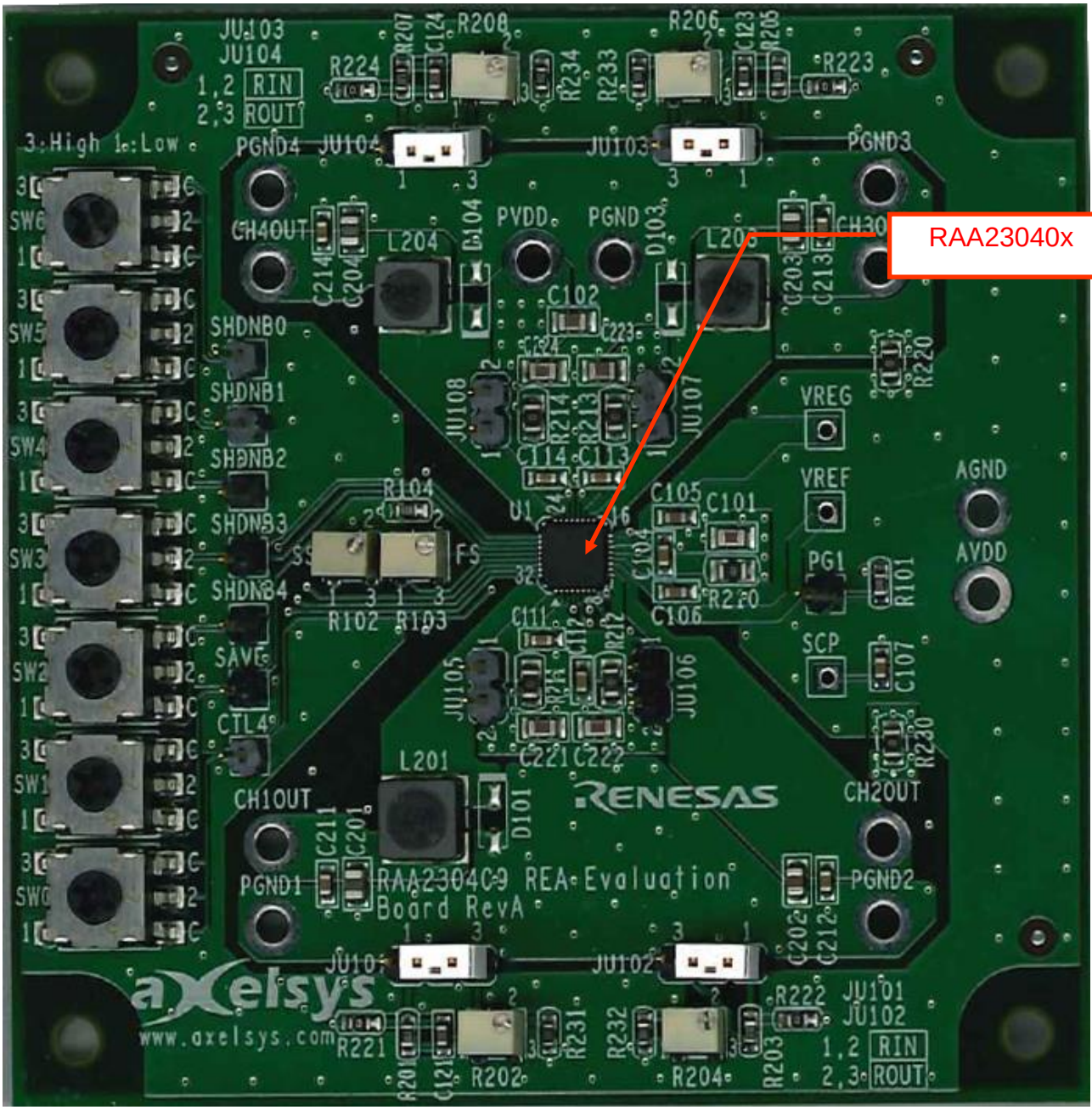
Note: RAA230409 is mounted on the evaluation board

Package Lineup

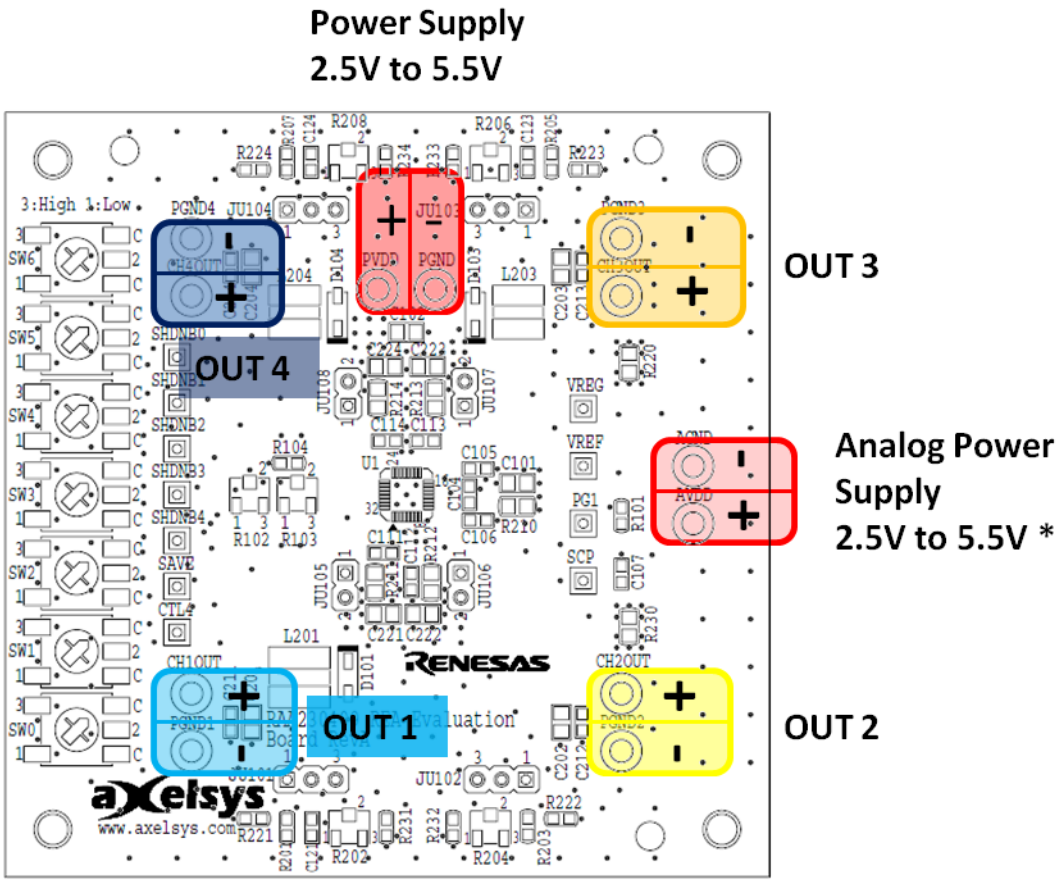
32-pin VQFN (PVQN0032LA-A)
32-pin LQFP (PLQP0032GB-A)

Note: 32-pin VQFN product is mounted on the evaluation board

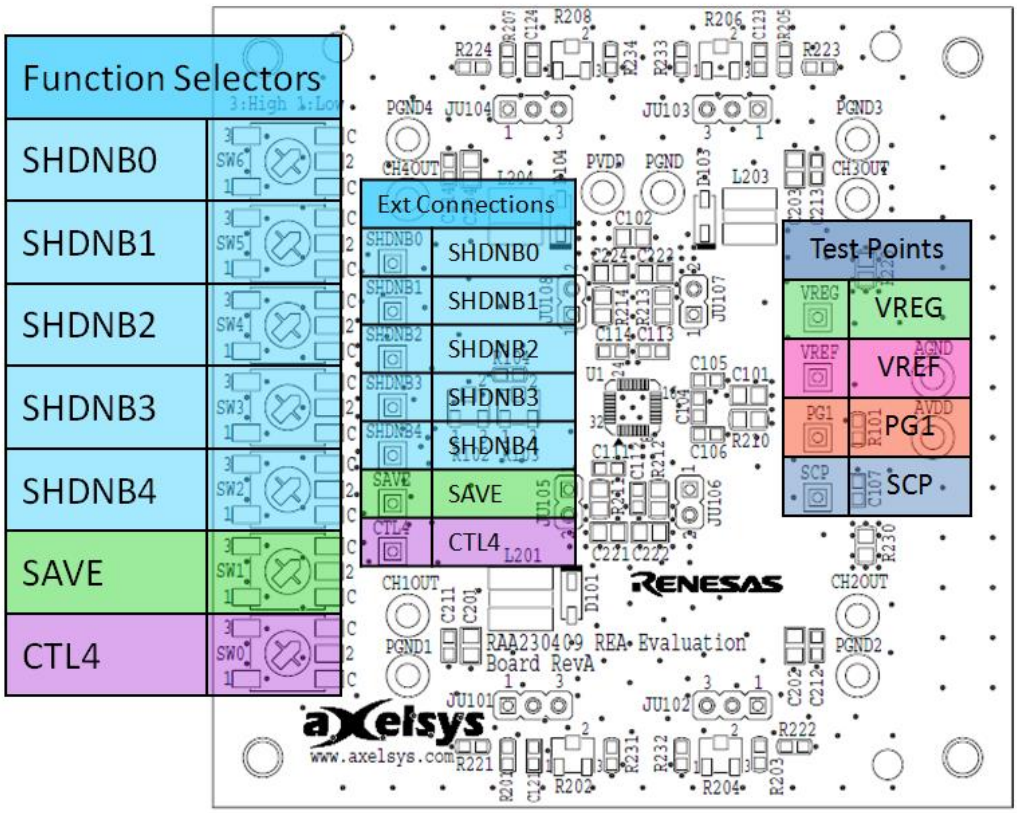
Photo of RAA230409 evaluation board

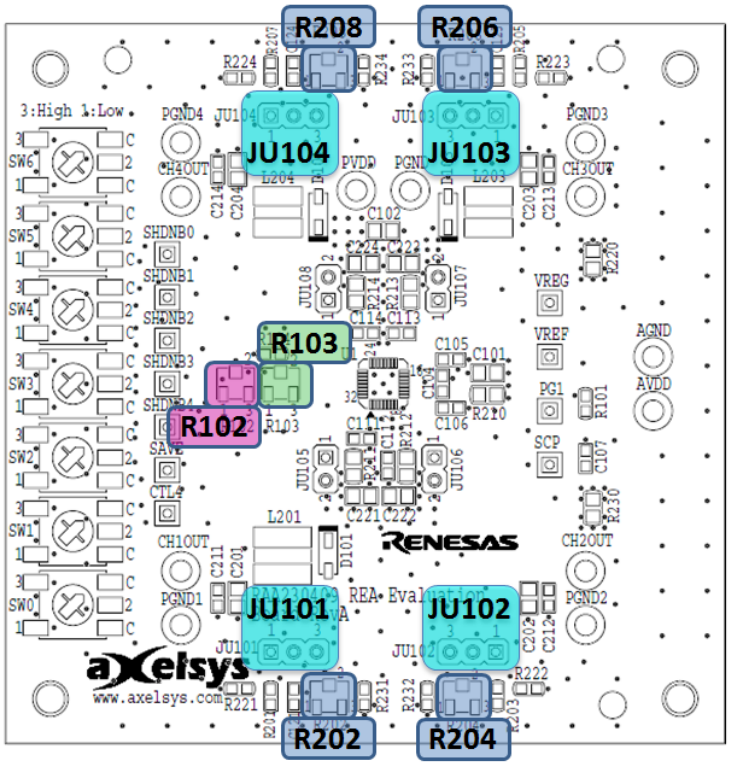


Connectors and Jumpers Description

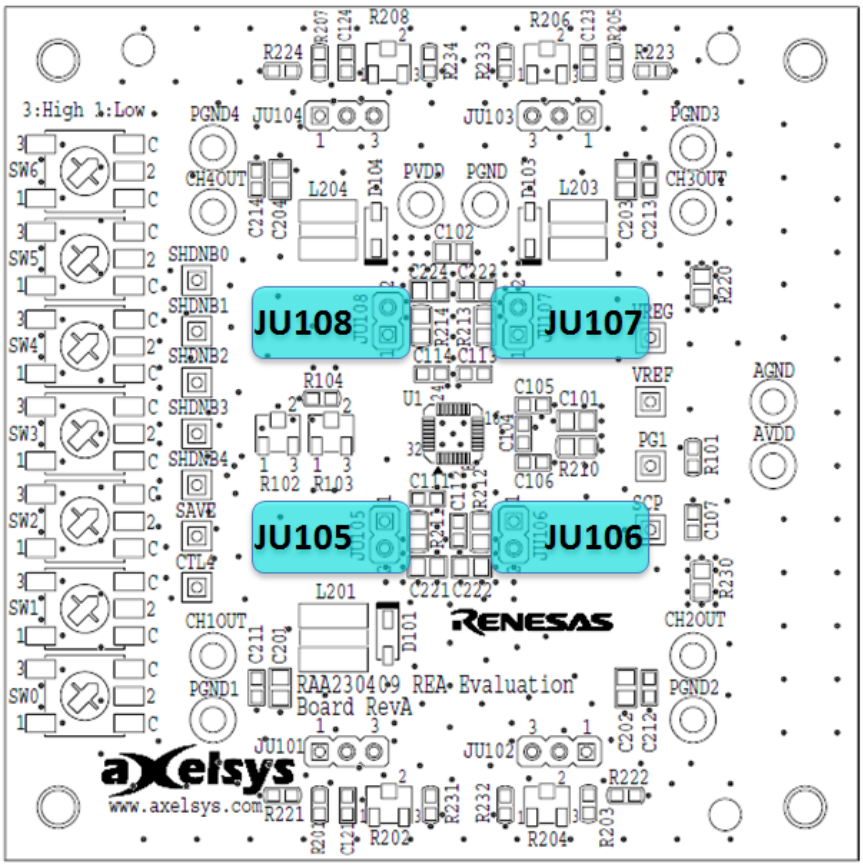


***not used (Connected to PVDD)**





R202-4-6-8	Output Voltage Trim
JU101-2-3-4	Output Voltage Selector
R102	Soft Start Trim
R103	SW Frequency Trim



JU105-6-7-8	Current Measurement Points

Jumpers Settings

JU101: selection of voltage setting circuit of CH1

JU101	Voltage setting circuit of CH1
1,2 RIN	Preset by internal resistor (for RAA230401~230408)
2,3 ROUT	Set by external resistors (for RAA230409)

JU102 : selection of voltage setting circuit of CH2

JU102	Voltage setting circuit of CH2
1,2 RIN	Preset by internal resistors (for RAA230401~230408)
2,3 ROUT	Set by external resistor (for RAA230409)

JU103 : selection of voltage setting circuit of CH3

JU103	Voltage setting circuit of CH3
1,2 RIN	Preset by internal resistors (for RAA230401~230404)
2,3 ROUT	Set by external resistor (for RAA230405~230409)

JU104 : selection of voltage setting circuit of CH4

JU104	Voltage setting circuit of CH4
1,2 RIN	Preset by internal resistors (1.2V output, when CTL4=High)
2,3 ROUT	Set by external resistor (when CTL4=Low)

JU105 : Input Current Measurement jumper for CH1 (if used, remove 0Ω resistor R211)

JU106 : Input Current Measurement jumper for CH2 (if used, remove 0Ω resistor R212)

JU107 : Input Current Measurement jumper for CH3 (if used, remove 0Ω resistor R213)

JU108 : Input Current Measurement jumper for CH4 (if used, remove 0Ω resistor R214)

Trimmers

R202: Output Voltage Adjust Trimmer for CH1

R204: Output Voltage Adjust Trimmer for CH2

R206: Output Voltage Adjust Trimmer for CH3

R208: Output Voltage Adjust Trimmer for CH4

Setting of Function Selectors switches

SW6 (setting of SHDNB0 pin) : On/Off of Common Circuit(VREF, VREG, oscillator, etc.)

SW6 (SHDNB0 pin)	Operation and status of Common Circuit
Low	OFF
Open	Set by external signal on monitor pin SHDNB0
High	ON

SW5 (setting of SHDNB1 pin) : On/Off of CH1

SW5 (SHDNB1 pin)	Operation and status of CH1
Low	OFF
Open	Set by external signal on monitor pin SHDNB1
High	ON

SW4 (setting of SHDNB2 pin) : On/Off of CH2

SW4 (SHDNB2 pin)	Operation and status of CH2
Low	OFF
Open	Set by external signal on monitor pin SHDNB2
High	ON

SW3 (setting of SHDNB3 pin) : On/Off of CH3

SW3(SHDNB3 pin)	Operation and status of CH3
Low	OFF
Open	Set by external signal on monitor pin SHDNB3
High	ON

SW2 (setting of SHDNB4 pin) : On/Off of CH4

SW2(SHDNB4 pin)	Operation and status of CH4
Low	OFF
Open	Set by external signal on monitor pin SHDNB4
High	ON

SW1 (setting of SAVE pin) selection of low-power mode

SW1 (SAVE pin)	Operation and status of IC
Low	Normal mode
Open	Set by external signal on monitor pin SAVE
High	Low-power mode

SW0 (setting of CTL4pin) : output voltage setting of CH4

SW0(CTL4 pin)	Setting of CH4 output voltage
Low	Set by external resistor
Open	Set by external signal on monitor pin CTL4
High	Preset by internal resistor (1.2V fixed output) (Remember to set JU104 to position 1-2)

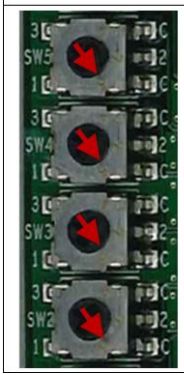
Board operation:

After connecting the power and make sure the voltage is within the admitted range (2.5V – 5.5V).

Make sure the Jumpers (JU101-4) are on ROUT position (2-3).

Enable the IC by turning SW6 to Position 3

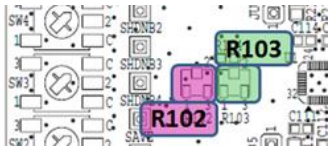
Enable individual channels (CH1-4) by turning the corresponding Switch (SW5-2) to position 3

	CHANNEL
	CH1
	CH2
	CH3
	CH4

To modify the output voltage of each channel, operate on the R202 (for CH1), R204 (CH2), R206 (CH3) and R208 (CH4).

To modify the Soft Start time, operate in R102.

To modify the Switching Frequency, operate on R103.

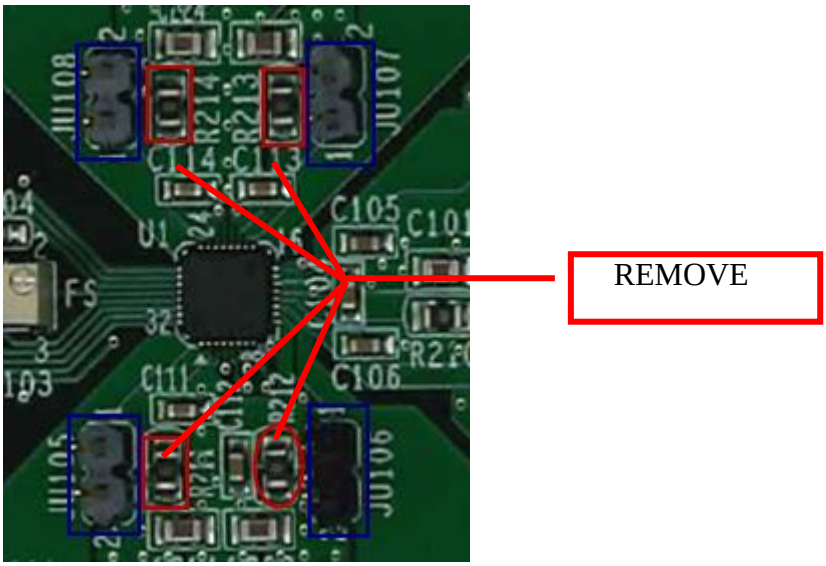


Input Current measurements:

The board allows precise input current measurements in 2 ways:

1. External current meter
2. External voltmeter and SHUNT resistor.

The use of a current meter is enabled by removing the 0Ω resistor corresponding to the selected channel (R211-214) and connecting the current meter on the jumper (JU105-108):



If a voltmeter is preferred, the 0Ω resistors need to be removed and a 0805 shunt need to be inserted; the following shunt values are suggested:

R211-212: 1Ω (1mV → 1mA)

R213-214: 100mΩ (1mV → 10mA)

NOTE1: for precise efficiency measurements, the input voltage should be measured on pin1 of the Jumpers, so that the voltage drop across the shunt resistor will not affect the measurement.

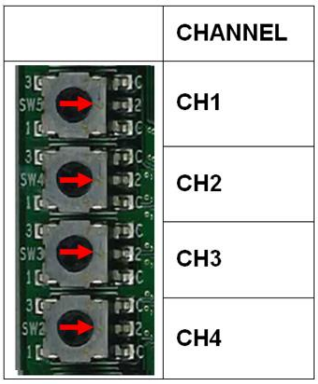
NOTE2: due to the voltage drop across the shunt or the current meter, make sure the NO-LOAD input voltage never exceeds 5.5V or use a power supply with remote sensing and connect the sense terminal to pin 1 of the current sensing jumpers.

Power-up sequencing

The evaluation board provides simple Power-on sequencing capabilities by using the SHDNB1-4 pins.

In order to use the SHDNB1-4 pins, the corresponding selector (SW5-2) must be put in position 2

In order to use one of the output rails as trigger for another rail, the output voltage of one rail will be connected to the corresponding SHDNB of the other rail.



For Example, if we want to implement the following sequence:

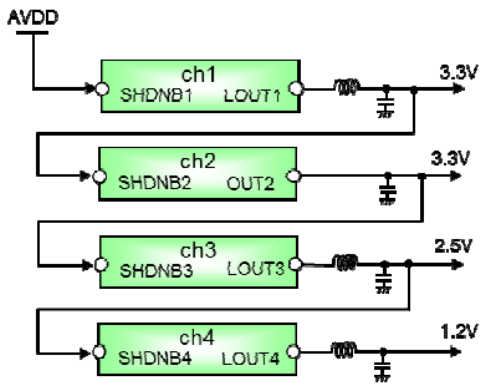
1. CH1: 3.3V
2. CH2: 3.3V
3. CH3: 2.5V
4. CH4: 1.2V

The following setup will be implemented:

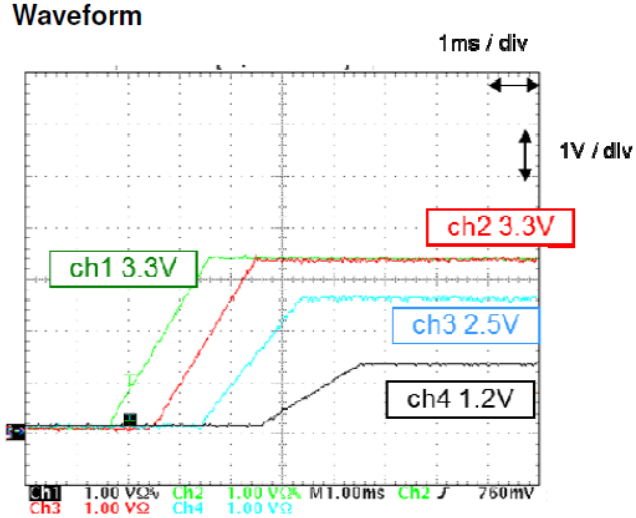
1. SHDNB1 connected to AVDD (SW5 in position 3)
2. CH1 Output connected to SHDNB2
3. CH2 Output connected to SHNDB3
4. CH3 Output connected to SHNDB4

See the connection diagram and the resulting Power-On Sequence below:

Configuration



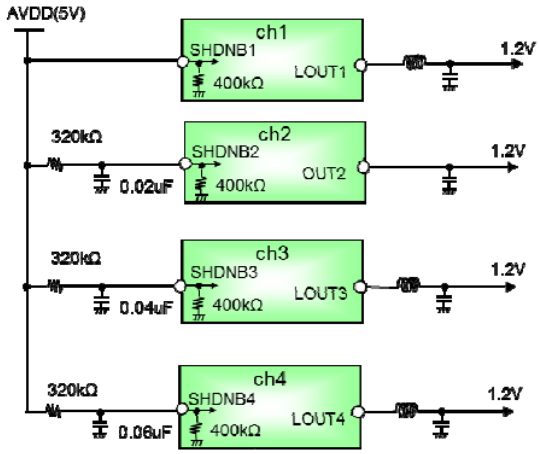
Waveform



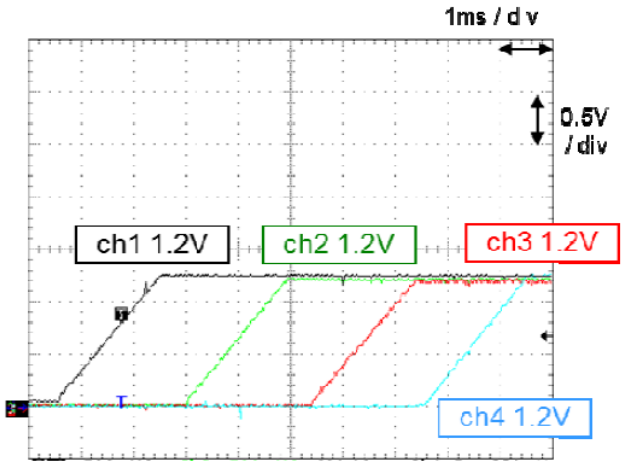
NOTE: The ON threshold (Vth) for SHDNBx pins can be anywhere between 0.8V and 2V so, in order to define the voltage at which the channel will be turn on, a voltage divider must be implemented, taking in account that SHDNBx pins have an internal 400kΩ pull-down resistor. As safety rule, Please make sure that input voltage divided by external resistor on SHDNB pins shall not be lower than 1.4V.

If the level of the controlling voltage is not enough to drive the SHDNBx pin, an RC network can be implemented to define the timing of the Power-on sequence, as per the following example:

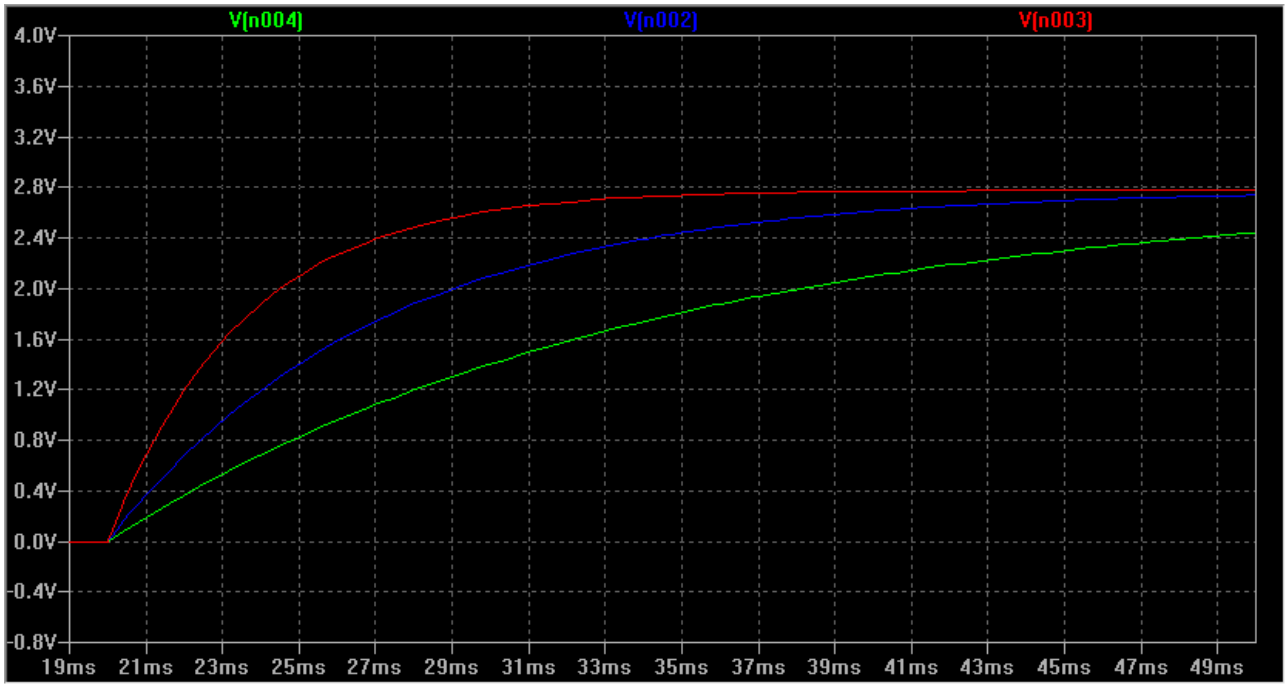
Configuration



Waveform



The time delay for this particular configuration can be seen in the simulation below:



Recommended Parts Spec

Input Capacitor

Recommended input capacitor of switching regulator can be calculated by the equation below. Use a capacitor with a value:

$$C_{IN} \geq \frac{I_{OUT}(MAX) \times \frac{V_{OUT}}{V_{IN}}}{\Delta V_{IN} \times f_{sw}}$$

For the LDO, connect the capacitor with a value greater than 1uF.

Please put the capasitor as close to the RAA23040x as possible, and shorten the distance between each power supply input pin and the ground.

Output Capacitor

Each channel of RAA23040x has a phase compensation circuit which is optimized for each operation. In order to ensure a stable operation with the phase compensation, we recommend the usage of an output capacitor of the following size:

- Switching Regulator (ch1, ch3, ch4): over 22uF
- LDO (ch2): over 2.2uF

Ceramic capacitors can be used as well: they have very low ESR, so VOUT ripple is greatly reduced.

VOUT ripple (ΔV_{rpl}) can be calculated by the equation below

$$\Delta V_{rpl} = \Delta IL \times \left(ESR + \frac{1}{(8 \times C_{OUT} \times f_{sw})} \right)$$

Inductor

It is recommended to choose an inductor which ripple current (ΔIL) results between 20 to 40 % of Iout(max).

When ΔIL increases, inductor current peak raises, so ripple of Vout gets larger and power losses increase. Conversely, large Inductors are required to lower ΔIL.

ΔIL can be calculated by an equation below.

$$\Delta IL = \frac{(Vin - Vout)}{L} \times \frac{Vout}{Vin} \times \frac{1}{f_{sw}}$$

(f_{sw}: Switching frequency, 1.3MHz to 2MHz)

Peak current of inductor (IL_{peak}) can be calculated by an equation below.

$$IL_{peak} = I_{out}(MAX) + \frac{\Delta IL}{2}$$

Choose a inductor which saturation current is higher than ILpeak . In addition, we recommend the following inductors according to the output current.

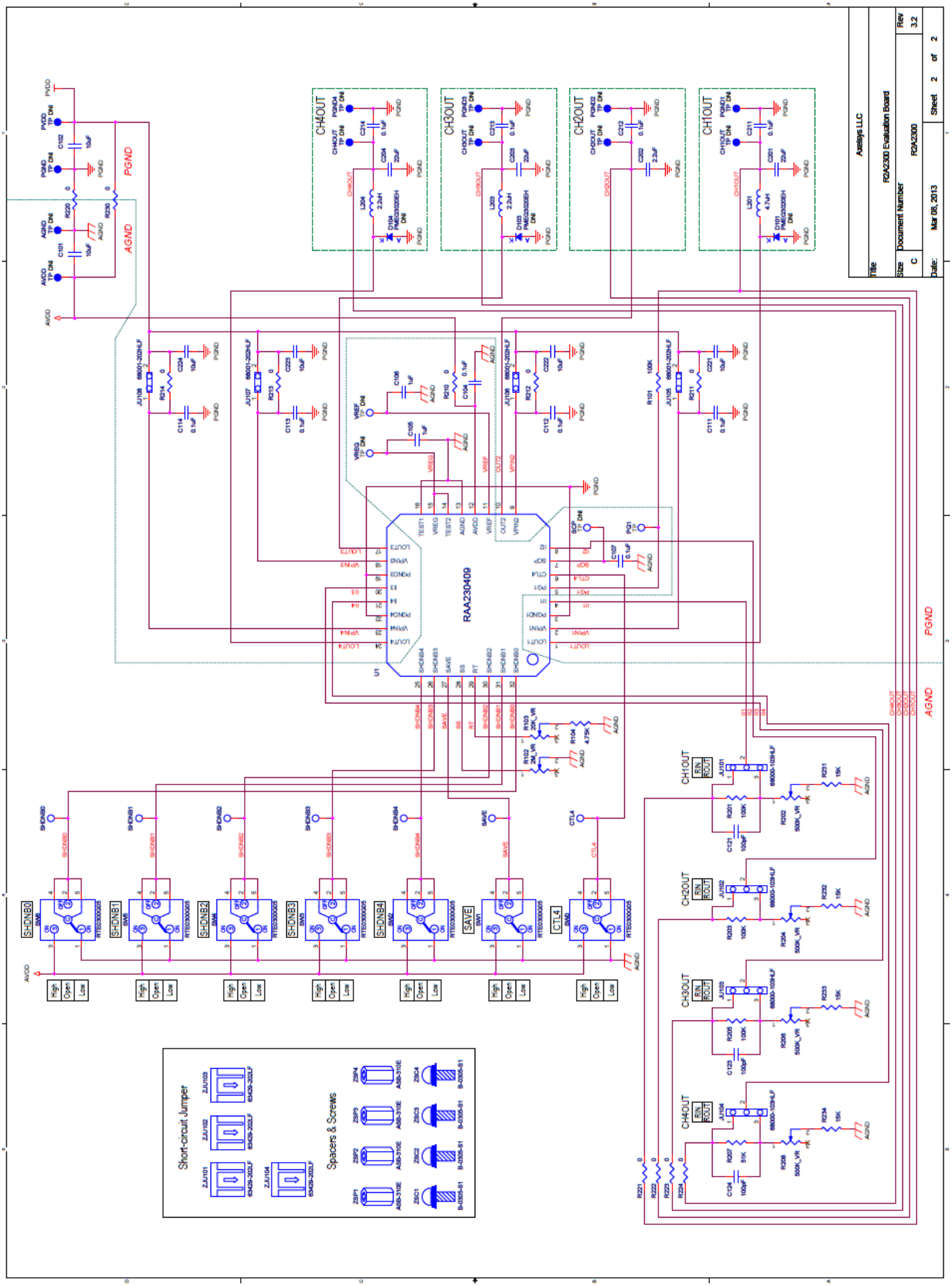
ch	Output Current	Inductor	Manufacturer	Inductance (uH)	I_{TEMP} (A)	I_{SAT} (A)	Size (LxWxT, mm)
ch1	less than 0.5A	CPL2512T4R7M	TDK	4.7	0.65	0.65	2.5x1.5x1.2
		NRS2012T4R7MGJ	TAIYO YUDEN	4.7	0.82	0.76	2x2x1.2
		74479787247A	WURTH	4.7	1.5	0.27	2.5x2x1
		744028004	WURTH	4.7	0.85	0.7	2.8x2.8x1.1
ch3 ch4	less than 1A	VLS201612ET-2R2M	TDK	2.2	1.15	1.05	2x1.6x1.2
		NRS2012T2R2MGJ	TAIYO YUDEN	2.2	1.37	1.35	2x2x1.2
		744029002	WURTH	2.2	1.5	1.15	2.8x2.8x1.35
	1A to 1.5A	LQH44PN2R2MP0	MURATA	2.2	1.8	2.5	4x4x1.65
		NRS4018T2R2MDGJ	TAIYO YUDEN	2.2	2.2	3	4x4x1.8
		744025002	WURTH	2.2	1.8	2.4	2.8x2.8x2.8

Note I_{TEMP} : Rated current by temperature rising
I_{SAT} : Rated current by inductance loss

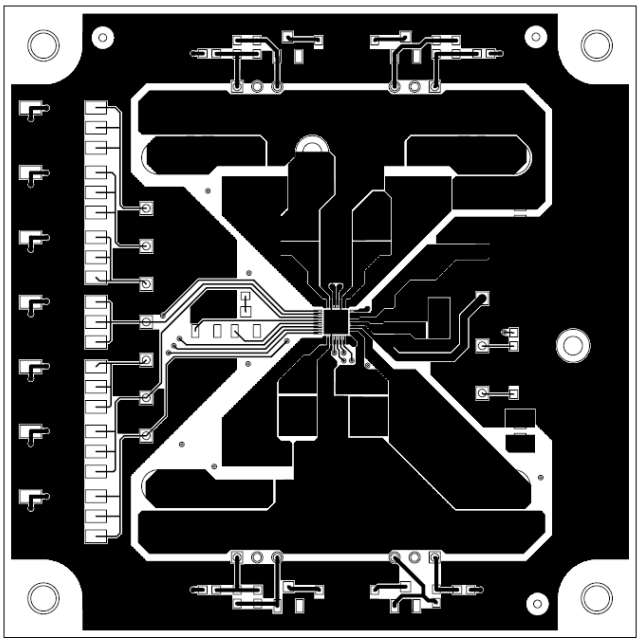
Efficiency Data

(Unless otherwise specified, T_A = 25°C, AV_{DD} = VP_{IN1} to VP_{IN4} = 5.0 V, f_{OSC} = 2 MHz)

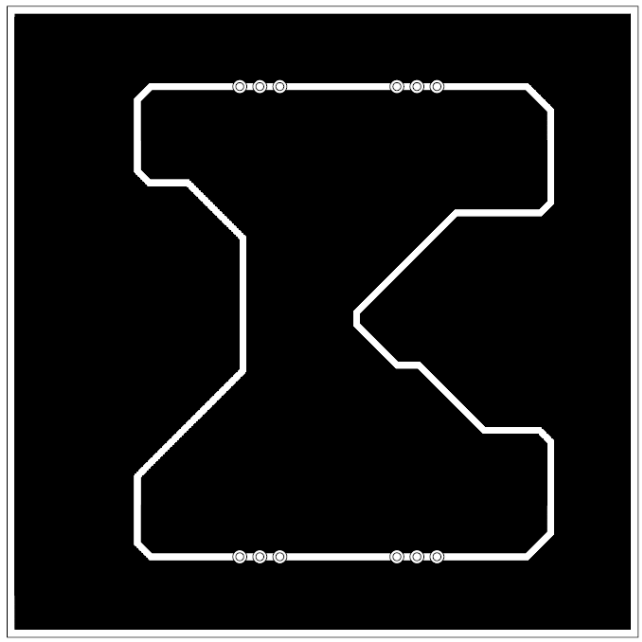
Schematic


RAA230409
U1
CH4OUT
CH3OUT
CH2OUT
CH1OUT
PGND
AGND
PVDD
AVDD
SHDNB0
SHDNB1
SHDNB2
SHDNB3
SHDNB4
SAVE
CTL4
Short-circuit Jumper
Spacers & Screws
Analogys LLC
R2A2300 Evaluation Board
R2A2300
Mar 08, 2013

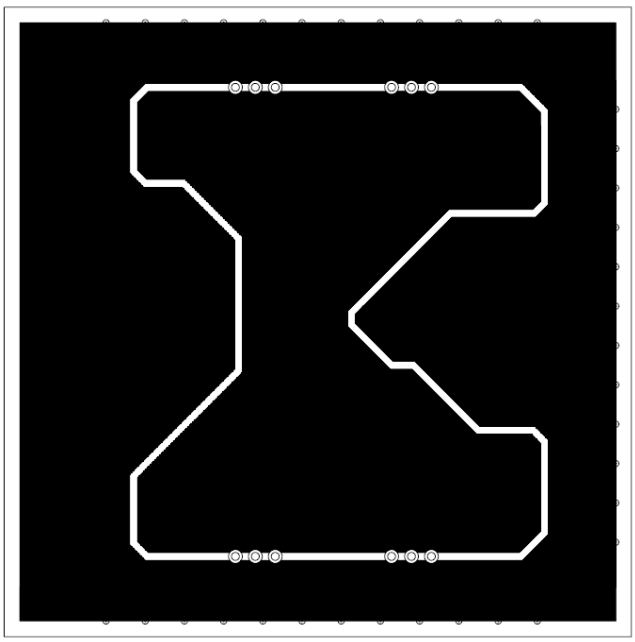
PCB LAYERS:



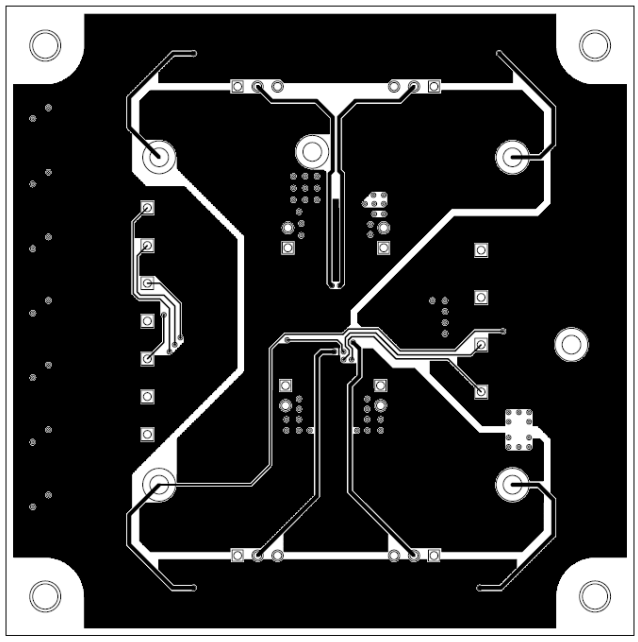
LAYER:01 TOP	COMPANY NAME: axelsys	
DESIGNER:LENNON WANG	PROJECT NAME: RAA230409 REA Evaluation Board	
CHECKER:LENNON WANG	PROJECT NUMBER: RAA230409	REV A
DATE:12MAR13		



LAYER:02 L2_GND	COMPANY NAME: axelsys	
DESIGNER:LENNON WANG	PROJECT NAME: RAA230409 REA Evaluation Board	
CHECKER:LENNON WANG	PROJECT NUMBER: RAA230409	REV A
DATE:12MAR13		



LAYER:03 L3_PWR	COMPANY NAME: axelsys	
DESIGNER:LENNON WANG	PROJECT NAME: RAA230409 REA Evaluation Board	
CHECKER:LENNON WANG	PROJECT NUMBER: RAA230409	REV A
DATE:12MAR13		



LAYER:4 BOTTOM	COMPANY NAME: axelsys	
DESIGNER:LENNON WANG	PROJECT NAME: RAA230409 REA Evaluation Board	
CHECKER:LENNON WANG	PROJECT NUMBER: RAA230409	REV A
DATE:12MAR13		

Note on Layout

At the layout design, separate the ground of the control signals from the ground of the power signals, so that these signals do not have common impedance as much as possible. In addition, lower the high-frequency impedance by using a capacitor, so that noise is not superimposed on the VREG pin and VREF pin.

Especially, the large current flows power supply input (VPIN), coil(LOUT), ground(PGND) of ch1, ch3 and ch4 by switching, so shorten and widen the line around those to lower line impedance.

Parts List

Qty	Reference	PART	Part	Part Number	Maker	Other P/N	other maker
1	U1	RAA23040x	CPU Power IC	RAA230409	Renesas		
3	D101,D103,D104	M1FM3	SMD_Schottky Diode_3918_30V/3A	M1FM3	Shindengen		
4	R221,R222,R223, R224	0_1608	Chip_resistor_1608_+/-5%	RK73Z1JTTD	KOA		
7	R210,R211,R212, R213,R214, R220,R230	0	Chip_resistor_2012_+/-5%	RK73Z2ATTD	KOA		
1	R207	51k	Chip_resistor_1608_+/-1%	RK73H1JTTD5102F	KOA	ERJ-3EKF5102V	Panasonic
4	R101,R201,R203, R205	100k	Chip_resistor_1608_+/-1%	RK73H1JTTD1003F	KOA	ERJ-3EKF1003V	Panasonic
1	R103	50k_VR	SMD_Cermet trimmer	SM-3W 50kΩ(503)	Copal Electronics		
4	R202,R204,R206, R208	200k_VR	SMD_Cermet trimmer	SM-3W 200kΩ(204)	Copal Electronics		
1	R102	2M_VR	SMD_Cermet trimmer	SM-3W 2MΩ(205)	Copal Electronics	3223W-1-205E	Bourns
3	C121,C123,C124	100pF	Chip Ceramic Capacitor_1608_50V_X7R	C1608X7R1H101K	TDK		
10	C104,C107,C111, C112,C113, C114,C211,C212, C213,C214	0.1uF	Chip Ceramic Capacitor_1608_100V_X7R	GRM188R72A104KA35D	muRata		
2	C105,C106	1uF	Chip Ceramic Capacitor_1608_25V_X7R	GRM188R71E105KA12D	muRata		
1	C202	2.2uF	Chip Ceramic Capacitor_2012_10V_X7R	GRM21BR71A225KA01L	muRata		
7	C101,C102,C103, C221,C222, C223,C224	10uF	Chip Ceramic Capacitor_3225_16V_X7R	GRM32DR71C106KA01L	muRata	GRM21BR61C106M E15	Murata
3	C201,C203,C204	22uF	Chip Ceramic Capacitor_3225_10V_X7R	GRM32ER71A226KE20L	muRata	GRM21BR61C226M E44	Murata
2	L203,L204	2.2uH	SMD_Inductor_5mm_±30%_4A	LQH5BPN2R2NT0	muRata	NRS4018T2R2MDGJ	TaiyoYuden
1	L201	4.7uH	SMD_Inductor_5mm_±30%_3A	LQH5BPN4R7NT0	muRata	NRS2012T4R7MGJ	TaiyoYuden
8	SW1,SW2,SW3,SW4 ,SW5,SW6, SW_TEST,SW0	G-13AP	Dip_Toggle SW	G-13AP	NKK		

D101, D103 and D104 are not mounted.

Website and Support

Renesas Electronics Website: www.renesas.com/

ICs for DC/DC Converter: http://am.renesas.com/SimpleDcDc

Eval Board Page: am.renesas.com/EVALRAA230

Inquiries: www.renesas.com/contact/

Ecosystem: www.renesasinteractive.com/

Revision Record

Rev.	Date	Description	
		Page	Summary
1	Aug 8, 2013	-	First English edition issued

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE: Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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