88PH8101

Field Programmable, High Voltage Synchronous Switching Regulator Controller

Datasheet

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Document Conventions

	**Note:** Provides related information or information of special importance.
	**Caution:** Indicates potential damage to hardware or software, or loss of data.
	**Warning:** Indicates a risk of personal injury.

Document Status

Doc Status: 2.00	Technical Publication: 0.xx

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PRODUCT OVERVIEW

The Marvell® 88PH8101 is a simple, easy to use synchronous switching regulator controller. A digital control algorithm provides a fast transient response and requires no external compensation components, minimizing the external component count. A feature unique with Marvell regulators is the ability to set the output voltage with either an external resistor, logic programmability, or serial interface.

Portable devices place tough design requirements on the power supply. To address these applications, the 88PH8101 operates as a fixed-frequency PWM when the load currents are high and automatically switches over to a pulse-skipping DCM mode at light loads. This characteristic results in high efficiency over a wide range of load currents.

Current limit utilizes the RDS(ON) of the upper MOSFET eliminating the need for a current sense resistor. Other key features of the 88PH8101 include soft start, short detection, under/over input voltage detection, diode emulation, forced PWM mode, adaptive dead time, and a power good signal.

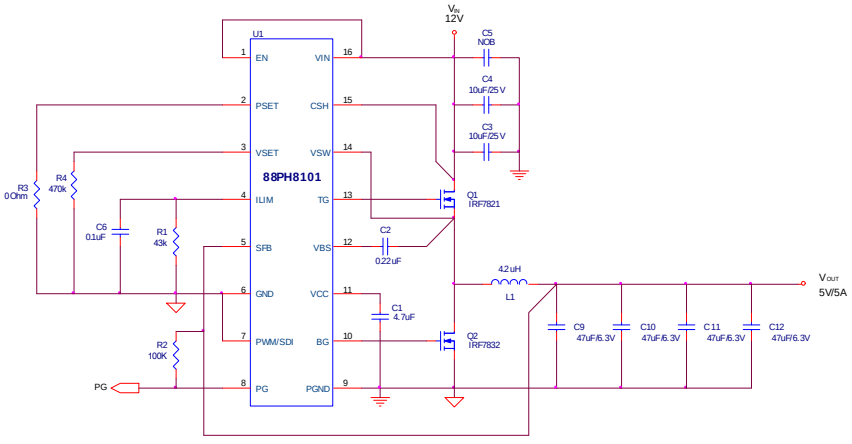
Features

- Operates from a 4.75V to 16V input
- Output voltage from 0.9V to 5.5V
- 500kHz switching frequency
- Stable with low-ESR ceramic output capacitors
- Up to 95% efficiency
- Drives N-channel MOSFETs
- Upper MOSFETs RDS (on) current limiting
- 2.5mA quiescent current (DCM-mode)
- Pre-bias Soft Start (DCM-Mode)
- Serial / Logic Programmability
- AnyVoltage™ Technology provides 72 output voltage selections to provide up most flexibility
- Input over voltage protection
- Output voltage margining capability
- Lead-free package
- TSSOP-16L package

Applications

- Point-of-load power supplies
- 12V PCI Express Bus

Figure 1: Typical Application Diagram for High Efficiency Step-Down Regulator



Caution!	**Caution:** This is a very high frequency device. Proper PCB layout is required. Section 6.1, PC Board Layout Considerations and Guidelines, on page 45.

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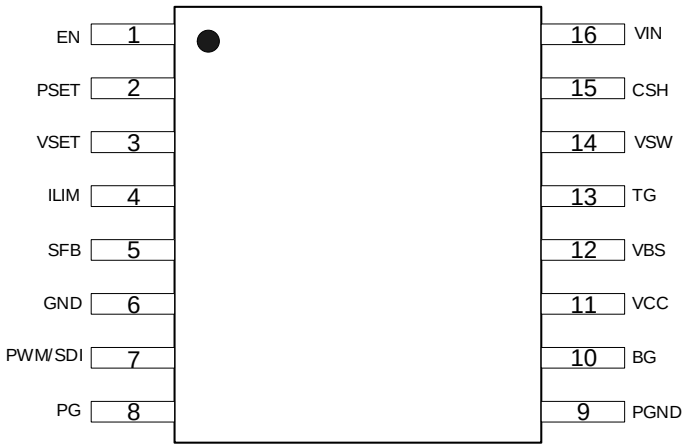
Figure 2: TSSOP-16 Diagram (Top View)



1.2 Pin Descriptions

Table 1: Pin Types

Pin Type	Definitions
I	Input Only
O	Output Only
S	Supply
NC	Not Connected
GND	Ground

Table 2: Pin Descriptions

Pin #	Pin Name	Pin Type	Pin Function
1	EN	I	Enable Logic high (≥ 2.0V) enables the regulator and logic low (≤ 0.8V) disables the regulator. If the pin is left floating, an internal 10 µA current source pulls this pin high to enable the regulator. (see Table 5, Electrical Characteristics, on page 16) Do not float this pin.
2	PSET	I	Percent Set 1. This is used for selecting the output voltage level when it is connected to GND or VCC in conjunction with VSET connection to GND or VCC. 2. Connect an external resistor to ground to set the output voltage of the step-down switching regulator. See Table 5, Electrical Characteristics, on page 16 for resistor values and Output Voltage Settings section. The total capacitance across this pin and GND should be equal to 25pF or less. Use resistor values with a tolerance of 5% tolerance or better. Do not float this pin.
3	VSET	I	Voltage Set 1. This is used for selecting the output voltage level, when it is connected to GND or VCC in conjunction with PSET connection GND or VCC. 2. Connect to an external resistor from VSET to GND to set eight nominal output voltages. See Table 11, Number of Voltage Steps for Each Output, on page 27. The total capacitance across this pin and GND should be equal to 25pF or less. Use resistor values with a tolerance of 5% tolerance or better. Do not float this pin.
4	ILIM	I	Current Limit Setting Point Connect a resistor to GND to set the peak current limit. ILIM = 0.2 * 20 µA * $R_{EXT}/RDS_{ON\ (Top\ FET)}$
5	SFB	I	Switch Regulator Output Voltage Sense Feedback Senses the output voltage of the switching regulator. Connect to the output capacitor of the switching regulator.
6	GND	GND	Signal Ground This pin must be connected to PGND and make a star connection to system ground.
7	PWM/ SDI	I	PWM / Serial Data Input 1. Logic high (≥ 2.0V) enables PWM mode operation and logic low (≤ 0.8V) to enable DCM mode operation at light loads. If the pin is left floating, an internal 10µA current source pulls this pin low, enabling DCM mode operation. 2. The input data into this pin is used to program the output voltage. See Section 3.4.2, Serial Programmability, on page 24. 3. Do not float this pin.
8	PG	O	Power Good (active high) This is an open-drain output that indicates the status of the output voltage. The output is pulled to ground when the output voltage is not within the specified tolerance. A 40µs falling edge de-glitch delay prevents tripping of the power good comparator due to high frequency noise.

Table 2: Pin Descriptions

Pin #	Pin Name	Pin Type	Pin Function
9	PGND	GND	Power Ground It must be connected to the negative terminals of the input and output capacitors.
10	BG	O	Gate drive for bottom MOSFET This pin drives the bottom MOSFET gate between 0V and VCC.
11	VCC	O	Internal 5V Regulator Output Place a ceramic capacitor close to this pin. • For 5V input operation, the internal LDO is one V_{TH} below V_{IN}. The internal LDO is not disabled. The VCC pin is connected to VIN for better efficiency.
12	VBS	I	Boot-Strap Voltage Node Place a ceramic capacitor as close as possible to the VBS and VSW pins.
13	TG	O	Gate drive for top MOSFET This pin drives the top MOSFET gate between 0V and V_{IN} + VCC
14	VSW	I	Switching Node This pin must be connected to the Source of top N-channel MOSFET using a Kelvin connection for more accurate current sensing.
15	CSH	I	High Side Current Sense Input This pin must be connected to the Drain of top N-channel MOSFET using a Kelvin connection for more accurate current sensing.
16	VIN	S	Internal LDO Input Power supply for internal LDO for generating VCC (5V).

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2 Electrical Specifications

2.1 Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings[1]

NOTE: Stresses above those listed in Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Parameter	Range	Units
V_{VIN} to GND	-0.3 to 20.0	V
PGND to GND	-0.3 to 0.3	V
V_{SW} to PGND[2]	-0.3 to (V_{IN} + 3.0)	V
V_{VCC} to GND	-0.3 to Minimum (V_{IN} + 0.3, 6.0)	V
V_{EN}, V_{CSH} to GND	-0.3 to V_{IN}	V
V_{VSET}, V_{PSET} to GND	-0.3 to 6.0	V
V_{SFB}, V_{PG}, $V_{PWM/SDI}$, V_{ILIM} to GND	-0.3 to 6.0	V
V_{BG} to PGND	-0.3 to 6.0	V
V_{TG} to V_{SW}	-0.3 to 6.0	V
V_{BS} to V_{SW}[3]	-0.3 to 6.0	V
Operating Ambient Temperature Range[4]	-40 to 85	°C
Maximum Junction Temperature	150	°C
Storage Temperature Range	-65 to 150	°C
Lead Temperature (soldering, 10s)	300	°C
ESD Rating[5] Human Body Model	2.0	kV

1. Exceeding the absolute maximum rating may damage the device.
2. Capable of -1.0V to (V_{IN} +0.3) for less than 50ns.
3. During normal operation, V_{BS} is periodically boosted to (V_{IN} + VCC). However, do not externally force the V_{BS} pin to more than (VCC + 0.3V).
4. Specifications over the -40°C to 85°C operating temperature ranges are assured by design, characterization and correlation with statistical process controls.
5. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5kΩ in series with 100pF.

2.2 Recommended Operating Conditions

Table 4: Recommended Operating Conditions[1]

Symbol	Parameter	Min	Typ	Max	Units
V_{VIN}	Input Voltage	4.75		16	V
θ_{JA}	Package Thermal Resistance[2]		86.3		°C/W
θ_{JC}			21.5		°C/W
T_{JMAX}	Maximum Operating Junction Temperature			125	°C

1. This device is not guaranteed to function outside the specified operating range.
2. Test on 4-layer (JESD51-7) and vias (JESD51-5) board.

2.3 Electrical Characteristics

Table 5: Electrical Characteristics

The following applies unless otherwise noted (refer to schematic shown in Figure 1): $V_{VIN} = V_{EN}$ =12V, V_{PFM} = GND, GND = PGND, V_{OUT} = 5V, L1 = 4.2µH, C1 = 4.7µF, C2 = 0.22µF, C3 = C4 = 10µF, C6 = 0.1µF, C9 = C10 = C11 = C12 = 47µF, T_A = 25°C. **Bold values indicate –40°C ≤ T_A ≤ 85°C.**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{VIN}	Input Voltage Range		**4.75**	12	**16**	V
I_Q	Total Quiescent Current (PFM Mode)	No load, V_{PWM} = 0V		2.5	**5.8**	mA
I_Q	Total Quiescent Current (PWM Mode)	No load, V_{PWM} = 5V		21	**40**	mA
I_{SHDN}	Shutdown Supply Current	V_{EN} = 0V, V_{VIN} = 12V		45	65	µA
V_{UVLO}	Under Voltage Lockout	High Threshold, V_{VIN} increasing		4.44	TBD	V
V_{UVLO}	Under Voltage Lockout	Low Threshold, V_{VIN} decreasing	TBD	4.35		V
V_{OVP}	Over Voltage Protection	High Threshold, V_{VIN} increasing		17.5	18.5	V
V_{OVP}	Over Voltage Protection	Low Threshold, V_{VIN} decreasing	16.5	16.7		V
T_{OTS}	Over Temperature Shutdown	T_J increasing (Disable regulators)		150		°C
T_{OTS}	Over Temperature Shut-down	T_J decreasing (Enable regulators)		100		°C
V_{IH}	EN and PWM Input Voltage Threshold	Logic high	2.0			V
V_{IL}	EN and PWM Input Voltage Threshold	Logic low			0.4	V
I_{EN}	Enable Input Current	V_{EN} = 12V			**1**	µA
I_{EN}	Enable Input Current	V_{EN} = 0V			**-10**	µA
I_{PWM}	PWM Input Current	V_{PWM} = 5V			**1**	µA
I_{PWM}	PWM Input Current	V_{PWM} = 0V			**1**	µA

2.3 Electrical Characteristics

Table 5: Electrical Characteristics

The following applies unless otherwise noted (refer to schematic shown in Figure 1): V_{VIN} = V_{EN} =12V, V_{PFM} = GND, GND = PGND, V_{OUT} = 5V, L1 = 4.2µH, C1 = 4.7µF, C2 = 0.22µF, C3 = C4 = 10µF, C6 = 0.1µF, C9 = C10 = C11 = C12 = 47µF, T_A = 25°C. **Bold values indicate –40°C ≤ T_A ≤ 85°C.**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{ILIM}	ILIM Pin Current			**-5**	**-10**	µA
	TC Current Limit	ILIM Temperature Coefficient		2000		ppm

2.4 Switching Step-down Regulator

Table 6: Switching Step-down Regulator

The following applies unless otherwise noted (refer to schematic shown in Figure 1): $V_{VIN} = V_{EN}$ =12V, V_{PFM} = GND, GND = PGND, V_{OUT} = 5V, L1 = 4.2µH, C1 = C9 = C10 = C11 = C12 = 4.7µF, C2 = 0.22µF, C3 = C4 = 10µF, C6 = 0.1µF, T_A = 25°C. **Bold values indicate –40°C ≤ T_A ≤ 85°C.**

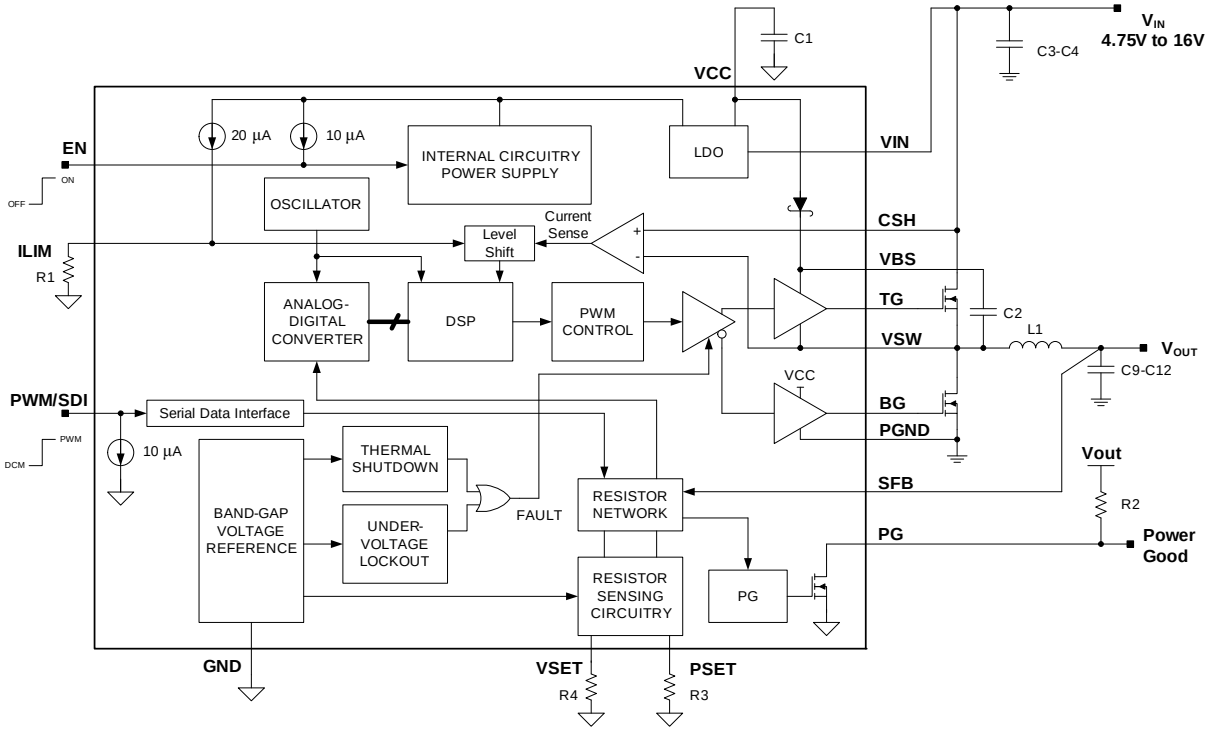
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OUT}	Output Voltage (PFM Mode)	R_{VSET} = 11K, PFM Mode, I_{LOAD} = 10mA		1.0		V
		R_{VSET} = 18K, PFM Mode, I_{LOAD} = 10mA		1.2		V
		R_{VSET} = 30K, PFM Mode, I_{LOAD} = 10mA		1.5		V
		R_{VSET} = 51K, PFM Mode, I_{LOAD} = 10mA		1.8		V
		R_{VSET} = 100K, PFM Mode, I_{LOAD} = 10mA		2.5		V
		V_{VSET} = 0V, V_{PSET} = 0V, PFM Mode, I_{LOAD} = 10mA				
		R_{VSET} = 160K, PFM Mode, I_{LOAD} = 10mA		3.0		V
		V_{VSET} = 0V, V_{PSET} = VCC, PFM Mode, I_{LOAD} = 10mA				
		R_{VSET} = 270K, PFM Mode, I_{LOAD} = 10mA		3.3		V
		V_{VSET} = VCC, V_{PSET} = 0V, PFM Mode, I_{LOAD} = 10mA				
		R_{VSET} = 470K, PFM Mode, I_{LOAD} = 10mA		5.0		V
		V_{VSET} = VCC, V_{PSET} = VCC, PFM Mode, I_{LOAD} = 10mA				

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OUT}	Output Voltage (PWM Mode)	R_{VSET} = 11K, PWM Mode, I_{LOAD} = 100mA		1.0		V
		T_A = 25°C	-3		+3	%
		R_{VSET} = 18K, PWM Mode, I_{LOAD} = 100mA		1.2		V
		T_A = 25°C	-3		+3	%
		R_{VSET} = 30K, PWM Mode, I_{LOAD} = 100mA		1.5		V
		T_A = 25°C	-2.5		+2.5	%
		R_{VSET} = 51K, PWM Mode, I_{LOAD} = 100mA		1.8		V
		T_A = 25°C	-2.5		+2.5	%
		R_{VSET} = 100K, PWM Mode, I_{LOAD} = 100mA		2.5		V
		V_{VSET} = 0V, V_{PSET} = 0V, PWM Mode, I_{LOAD} = 100mA				
		T_A = 25°C	-2		+2	%
		R_{VSET} = 160K, PWM Mode, I_{LOAD} = 100mA		3.0		V
		V_{VSET} = 0V, V_{PSET} = VCC, PWM Mode, I_{LOAD} = 100mA				
		T_A = 25°C	-2		+2	%
		R_{VSET} = 270K, PWM Mode, I_{LOAD} = 100mA		3.3		V
		V_{VSET} = VCC, V_{PSET} = 0V, PWM Mode, I_{LOAD} = 100mA				
		T_A = 25°C	-2		+2	%
		R_{VSET} = 470K, PWM Mode, I_{LOAD} = 100mA		5.0		V
		V_{VSET} = VCC, V_{PSET} = VCC, PWM Mode, I_{LOAD} = 100mA				
		T_A = 25°C	-2		+2	%
P_{SET}	Percentage Set	R_{PSET} = 11K		-10.0		%
P_{SET}	Percentage Set	R_{PSET}= 18K		-7.5		%
P_{SET}	Percentage Set	R_{PSET} = 30K		-5.0		%
P_{SET}	Percentage Set	R_{PSET} = 51K		-2.5		%
P_{SET}	Percentage Set	R_{PSET} = 0K		0		%
P_{SET}	Percentage Set	R_{PSET} = 100K		2.5		%
P_{SET}	Percentage Set	R_{PSET} = 160K		5.0		%
P_{SET}	Percentage Set	R_{PSET} = 270K		7.5		%
P_{SET}	Percentage Set	R_{PSET} = 470K		10.0		%

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{LNREG}	Output Voltage Line Regulation	V_{VIN} = 9V to 12V, I_{LOAD} = 2.5A		0.01		%
V_{LDREG}	Output Voltage Load Regulation	V_{VIN} = 12V, I_{LOAD} = 2.5A to 5A		0.1		%
f_{SW}	Switching Frequency		400	500	600	kHz
D_{MAX}	Maximum Duty Cycle			90		%
$t_{DEGLITCH}$	Deglitch			40		µs
V_{PGTH}	Power Good (PG) Threshold Voltage	$V_{OUT} \geq$ 1.35V		V_{OUT} × 90%		V
V_{PGTH}	Power Good (PG) Threshold Voltage	V_{OUT} < 1.32V		V_{OUT} – 130mV		V
V_{PGL}	Maximum PG Output Low Voltage	I_{SINK} = 1mA			0.4	V
t_{DELAY}	PG Delay Time			512		µs
I_{PG}	PG Leakage Current	V_{EN} = 5.0V		1	20	µA
t_{DNV}	Driver Non Overlap	C_L = 3300 pF		30		ns
t_R, t_F	Driver Rise/Fall Time	C_L = 3300 pF		15		ns
R_{SOURCE}	Output Driver Impedance Top Driver			1.5	3	Ω
R_{SINK}	Output Driver Impedance Top Driver			1.0	2.5	Ω
R_{SOURCE}	Output Driver Impedance Bottom Driver			1.5	4.2	Ω
R_{SINK}	Output Driver Impedance Bottom Driver			0.5	2.5	Ω

3 Functional Description

Figure 3: Block Diagram



3.1 Overview

The 88PH8101 incorporates a new controller architecture that minimizes the number of external passive components, improves efficiency and provides fast transient response. A non-linear control algorithm is able to detect and react to severe load changes in less than 100 ns and requires no external compensation components, reducing design time. Efficiency is improved by having an adaptive dead time control that reduces the on time of the parasitic diode of the low-side MOSFET. Lossless switch current sensing utilizes the RDS (ON) of the high-side MOSFET to eliminate the need for a current sense resistor, improving efficiency. Other features include under and over voltage lockout, over temperature shutdown, power good detection, and cycle-by-cycle current limiting.

Additionally, there are 3 simple ways to set the output voltage using external resistors, logic control or a serial interface. External resistors connected to the VSET and PSET pins are measured once before start up. These 2 resistors provide up to 72 output voltage options from 0.9V to 5.5V. These external resistors can be eliminated by tying the VSET and PSET pin high or low, generating 2.5V, 3.0V, 3.3V or 5.0V.

Some applications require voltage margining, forcing the output voltage a percentage above and below its nominal value. In this case, the serial interface can be used to change the output ±0%, ±2.5%, ±5.0%, ±7.5%, ±10% or any one of the 72 voltage options.

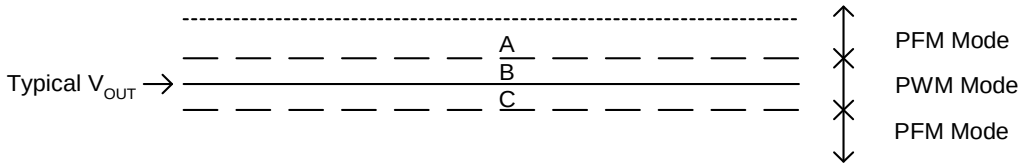
To address portable applications, the 88PH8101 operates as a fixed frequency PWM when the load currents are high and automatically switches over to pulse skipping DCM mode at light loads, reducing no-load supply current from 21 mA to 2.5mA. For DDR applications where the converter must source and sink current, the PWM pin can be tied high, forcing PWM mode under all output current conditions.

3.2 Regulation and Start-up

The step-down switching regulator can operate in Pulse Width Modulation Mode (PWM), Discontinuous Current Operating Mode (DCM), or Pulse Frequency Mode (PFM). The mode of operation depends on the level of output current and the output voltage.

In steady states, the step-down switching regulator monitors the current flowing through the inductor to determine if the regulator is handling a heavy or light load. For heavy loads, the step-down regulator operates in the PWM mode (B) to minimize the ripple current for optimum efficiency and to minimize the ripple output voltage. The step-down regulator automatically switches over to pulse frequency (PFM) mode (A) at light loads for optimum efficiency in light load applications. In this mode, the average output voltage is slightly higher than the average output voltage when operating in PWM mode. In over current conditions and during start up, the regulator operates in PFM mode (C).

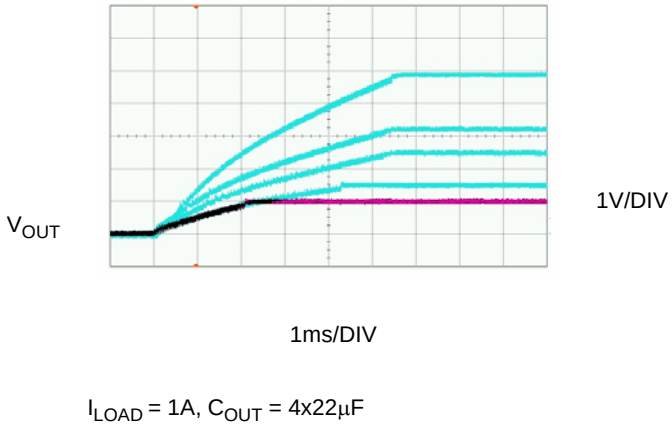
Figure 4: Output Voltage Window



3.3 Soft Start

Soft start is a highly desirable property in “Hot-Plug” applications. It limits the large inrush currents on the input power supply during start up. The 88PH8101 device controls the rise time of the output voltage, thereby dramatically reducing the inrush current. The rise time is tyically 5ms for VOUT higher than 1.65V and 0.33V/ms for VOUT ≤ 1.65V and it is independent of output capacitance and load current. Figure 5 shows the rise time for various output voltage settings.

Figure 5: Soft Startup (1V, 1.5V, 2.5V, 3.3V, 5V)



3.4 Output Voltage Setting

3.4.1 Logic Programmability

The output voltage of the step-down switching regulator can be programmed for the standard output voltages by connecting VSET and PSET pins to GND and/or VCC. This method will eliminate the use of external resistor to set the output voltage.

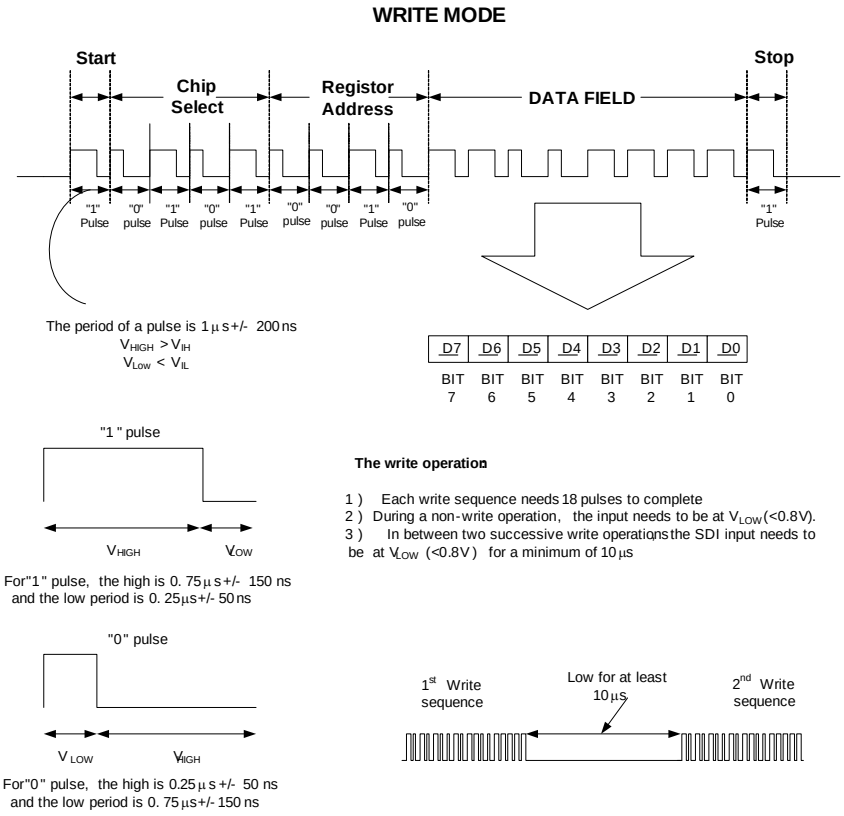
Table 7: Output Voltage Setting

V_{VSET}	V_{PSET}	V_{OUT}
GND	GND	2.5V
GND	VCC	3.0V
VCC	GND	3.3V
VCC	VCC	5.0V

3.4.2 Serial Programmability

The output voltage of the step-down switching regulator can also be programmed by using 18-bit serial data into the SDI pin.

Figure 6: Serial Programmability



The first 4 bits (MSB) of the data field are used to select the output voltage where the second 4 bits (LSB) of the data field are used to trim the output voltage (percent of output voltage). The default value for the data field is as follows:

Table 8: Default Value of Data Field

	Data Field							
Description	**Voltage Set**				**Percent Set**			
Bits	7	6	5	4	3	2	1	0
Default value	0	0	1	0	0	1	0	0

The value for position 7 and 3 of the register will enable use of either logic or serial output voltage programmability. Bit value of “0” for positions 7 and 3 will enable the resistor/logic programmability and the output voltage will be set according to Section 3.4.1 A bit value of “1” will enable the serial programmability. The output voltage and percent set are selected per following table:

Table 9: Voltage and Percent Set

	Data Field				VOUT (V)	Data Field				Percent Set
Bits	**7**	**6**	**5**	**4**		**3**	**2**	**1**	**0**	
Value	1	0	0	0	1.0	1	0	0	0	-10%
	1	0	0	1	1.2	1	0	0	1	-7.5%
	1	0	1	0	1.5	1	0	1	0	-5.0%
	1	0	1	1	1.8	1	0	1	1	-2.5%
	1	1	0	0	2.5	1	1	0	0	+2.5%
	1	1	0	1	3.0	1	1	0	1	+5.0%
	1	1	1	0	3.3	1	1	1	0	+7.5%
	1	1	1	1	5.0	1	1	1	1	+10%

All combinations of the Voltage Set and Percentage Set provide flexability in output voltage selection, as shown in Table 9.

3.5 Output Voltage—AnyVoltage™ Technology

The output voltage of the step-down switching regulator is programmed by using Table 10 to select resistor values for VSET and PSET pin. The VSET pin sets the output voltage and the PSET pin trims the set voltage to a percentage value. For example, to program 2.25V output, a 100 kΩ resistor is selected for the VSET pin, and an 11 kΩ resistor is selected for the PSET pin. The 100 kΩ resistor sets the output voltage to 2.5V and the 11 kΩ resistor trims the set voltage by -10%.

Using the VSET resistor's value greater than 619 kΩ or less than 7.68 kΩ disables the step-down switching regulator and sets the SW pin to high impedance. If the VSET resistor's value is outside the 5% tolerance, the output can be either higher or lower than the set voltage.

Using resistor values greater than 619 kΩ or less than 7.68 kΩ for the PSET pin does not affect the set voltage. When the PSET pin is not used, it must be connected to ground. Like the VSET resistor, the percent value is either higher or lower if the PSET resistor's value is outside the 5% tolerance.

Table 10: VSET and PSET Programming Table for 5% Resistors

		Percentage Set (%)								
		-10.00%	-7.50%	-5.00%	-2.50%	0%	2.50%	5.00%	7.50%	10%
		11K	18K	30K	51K	GND	100K	160K	270K	470K
Voltage Set (V)	11K	0.900	0.925	0.950	0.975	1.00	1.025	1.050	1.075	1.100
	18K	1.080	1.110	1.140	1.170	1.20	1.230	1.260	1.290	1.320
	30K	1.350	1.388	1.425	1.463	1.50	1.538	1.575	1.613	1.650
	51K	1.620	1.665	1.710	1.755	1.80	1.845	1.890	1.935	1.980
	100K	2.250	2.313	2.375	2.438	2.50	2.563	2.625	2.688	2.750
	160K	2.700	2.775	2.850	2.925	3.00	3.075	3.150	3.225	3.300
	270K	2.970	3.053	3.135	3.218	3.30	3.383	3.465	3.548	3.630
	470K	4.500	4.625	4.750	4.875	5.00	5.125	5.250	5.375	5.500

The VSET and PSET resistors are read once during start-up before the output voltage is turned on. After the output voltage is turned on, the output voltage can change to different values using serial programming interface. Otherwise to configure the output to a different voltage, power has to recycle or the 88PH8101 has to turn OFF and back ON using the enable pin.

Figure 7 shows the startup waveforms of the 88PH8101. Once the input voltage (V_{IN}) is above the under voltage lockout (UVLO) upper threshold (UTH), the VSET and PSET pin become active. Current is first sourced out of PSET pin and then the VSET pin, in exponentially increasing steps. After each step there is a blanking time before the VSET voltage is compared to an internal 1.2V reference. If the VSET voltage is below internal reference voltage and the current source proceeds to the next set. Once the VSET voltage is above the internal reference voltage the sequence stops and the output voltage (VOUT) is allowed to turn-on. Figure 7 shows the VSET waveform for VSET = 2.5V and PSET = –5% output in low-voltage mode. The 88PH8101 keeps track of how many steps were required to determine the appropriate output voltage. Table 11 provides the number of steps necessary for each output voltage option. Using a VSET resistor of 100kΩ requires the current source to step 5 times, and a PSET resistor of 30 kΩ requires 7 steps.

Figure 7: Startup Sequence

Figure 8: Soft Startup

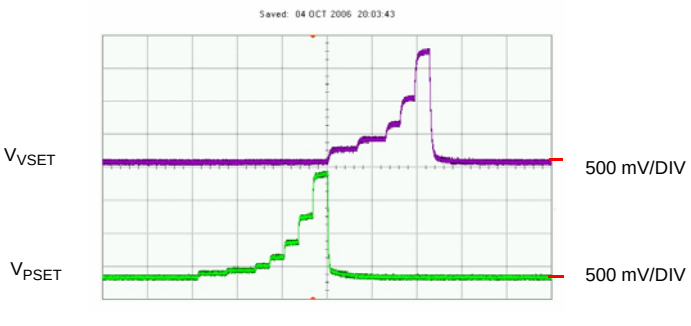


Table 11: Number of Voltage Steps for Each Output

Step	V_{OUT} (V)	R_{VSET} (kΩ)
1	0	0
2	5.0	470
3	3.3	270
4	3.0	160
5	2.5	100
6	1.8	51
7	1.5	30
8	1.2	18
9	1.0	11

Step	P_{SET} (%)	R_{PSET} (kΩ)
1	0	0
2	+10	470
3	+7.5	270
4	+5.0	160
5	+2.5	100
6	-2.5	51
7	-5.0	30
8	-7.5	18
9	-10	11

The 88PH8101 provides an innovative technique to set the output voltage. During start-up it reads the value of external resistors, which are located outside the regulator's feedback loop, to program the output voltage. By placing the output voltage programming resistor outside the regulator's feedback loop, its tolerance does not affect the accuracy of the output voltage. While in conventional designs, adjustable regulators use 1% resistors to set the output voltage. However, these resistors are located inside the feedback loop, introducing as much as 2% of initial accuracy error to the output voltage, resulting in an overall initial accuracy of 3%. Whereas, the 88PH8101 initial accuracy is 2% for any of the eight output voltages.

The VSET and PSET pins are sensitive to excessive leakage currents and stray capacitance. The output voltage can potentially be programmed to the lower output voltage if there is contamination, which introduces excessive leakage current on the VSET and PSET pin, especially for a R_{VSET} and R_{PSET} of 470kΩ. The parasitic resistance on these nodes must be greater than 3MΩ and the stray capacitance must be less than 25pF; otherwise, a 5.0V output can potential end up at 3.3V in low-voltage mode.

3.6 Thermal Shutdown

When the junction temperature of the 88PH8101 exceeds OTS high threshold, the thermal shutdown circuitry disables the step-down regulator. The step-down switching regulator is enabled when the junction temperature is decreased to OTS low threshold.

3.7 PFM or PWM Mode Selection

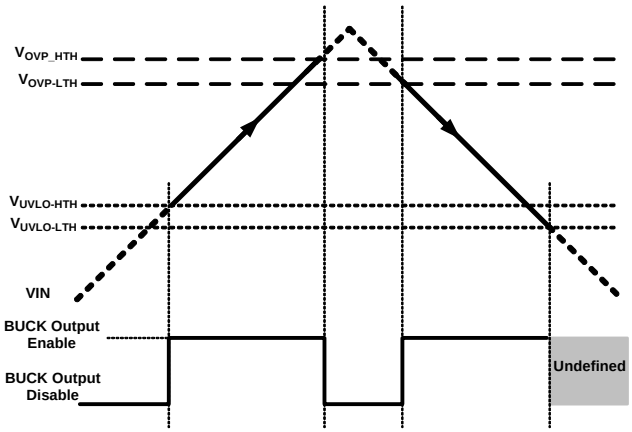
When PFM pin is connected to high state, the regulator is in the forced PWM mode, where the regulator runs at a constant frequency. The quiescent current of the forced PWM mode increases to 21mA (typical). When PFM pin is connected to a low state, the regulator runs in PFM mode, where the switching frequency decreases when the load current reduces, thus improving the light load efficiency.

3.8 Under Voltage Lockout (UVLO)

The Under Voltage Lockout (UVLO) feature insures that both MOSFETs have adequate voltage levels to operate properly. When the input voltage drops below UVLO low threshold, both MOSFETs are off until the input rises above UVLO high threshold. See Section 2.3 for the UVLO low and high threshold voltages.

3.9 Over Voltage Protection (OVP)

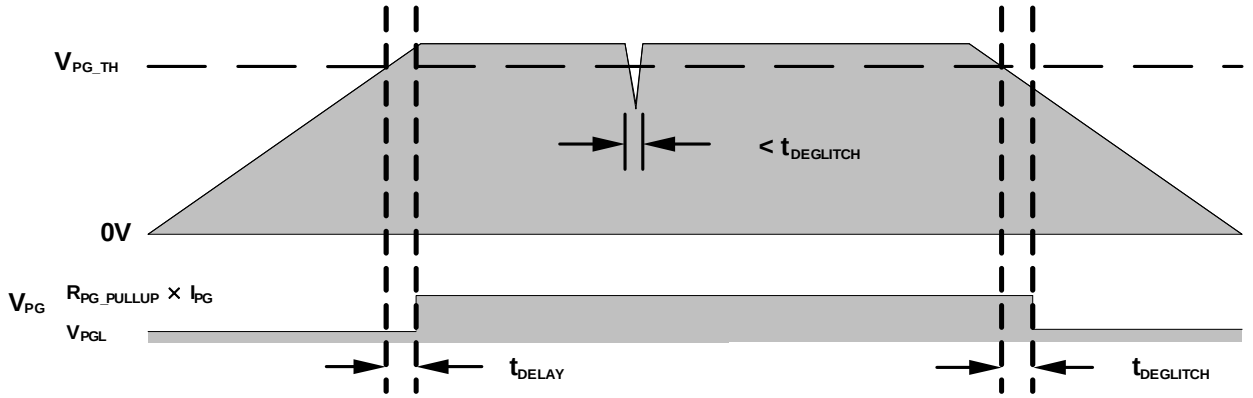
For Over Voltage Protection (OVP), an over voltage comparator guards against transient overshoots, as well as other serious conditions, that may damage the IC. When the input voltage is above the OVP high threshold voltage, both external high-side N-channel MOSFET are turned off until the input voltage drops below the OVP low threshold voltage. See section 2.3 for the OVP low and high voltages..



3.10 Power Good (PG)

The Power Good (PG) pin is an active-high, open-drain output pin. It is low when the output voltage of the step-down regulator is below the threshold. When the output voltage is above the threshold for more than 512µs (t_{DELAY}), the power good pin goes high. The threshold voltage is 0.9% * V_{OUT} (typical) for all output voltage settings. A built-in $t_{DEGLITCH}$ (40µs typical) delay is incorporated to prevent nuisance tripping.

Figure 9: Power Good Operating Waveform



3.11 Hiccup Current Limit

The “Hiccup“ short-circuit protection is a feature that is not common among other switching regulators. Hiccup mode offers extra protection against over current situations, since it limits the average current to the load, reducing power dissipation and case temperature of the IC. When the current-sense circuit sees an over-current condition together with a low output voltage condition (VOUT < 75% nominal), the 88PH8101 device shuts off for about 2ms and then tries to start up again. If the over-load condition is removed, the devices will start-up normally; otherwise, the IC will see another over-current event and shut off once again, repeating the previous cycle.

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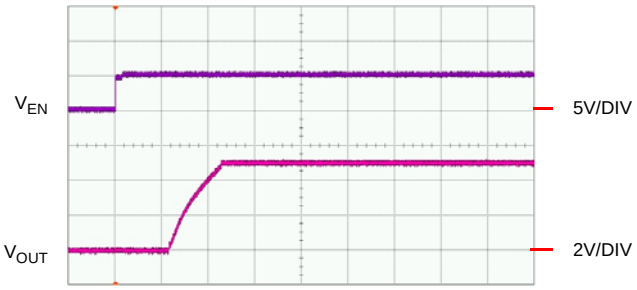
4 Functional Characteristics

Unless otherwise noted, the following typical scope photographs were taken using test circuit shown in figure 1 at T_A = 25°C.

4.1 Startup Waveforms

NOTE: When the input voltage rises above the UVLO's upper threshold, then there is a delay (4ms typ) before the step-down regulator's output voltage powers on.

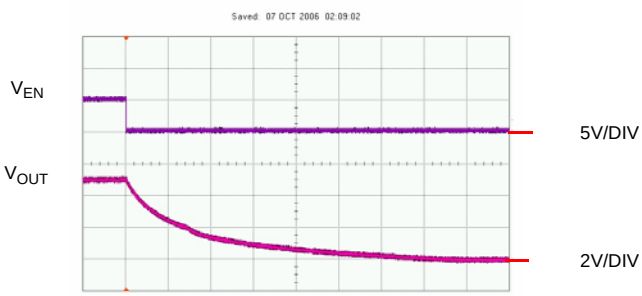
Figure 10: Startup Using the Enable Pin



V_{IN} = 12V I_{LOAD} = 10mA

V_{OUT} = 5V

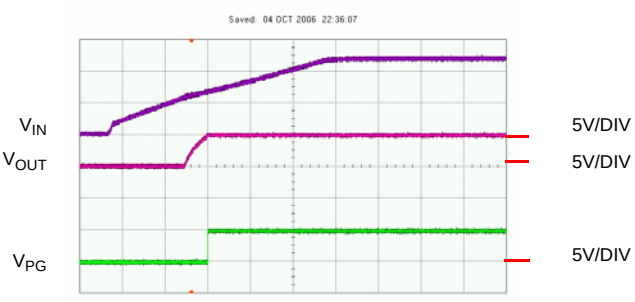
Figure 11: Turn Off Using the Enable Pin



V_{IN} = 12V I_{LOAD} = 10mA

V_{OUT} = 5V

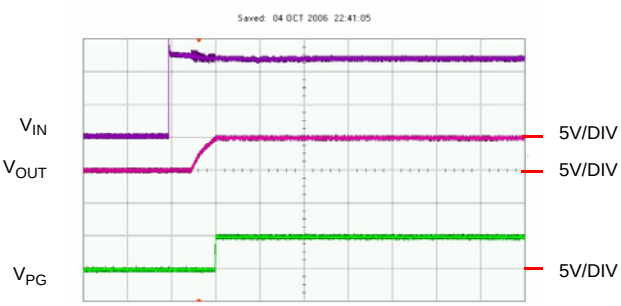
Figure 12: Soft Start



V_{IN} = 12V I_{LOAD} = No Load

V_{OUT} = 5V

Figure 13: Hot Plug



V_{IN} = 12V I_{LOAD} = No Load

V_{OUT} = 5V

4.2 Switching Waveforms

NOTE: For repeatability of measuring output ripple ($V_{OUT\ (P-P)}$) for the BUCK regulator, the standard test procedure limits the scope bandwidth to 20MHz and uses a coax cable with very short leads terminated into 50Ω. The coax leads must be routed away from the switching node as much as possible.

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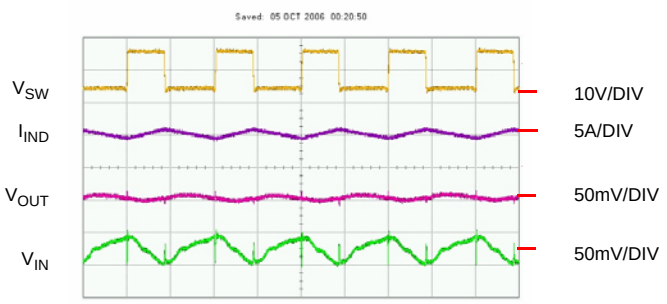
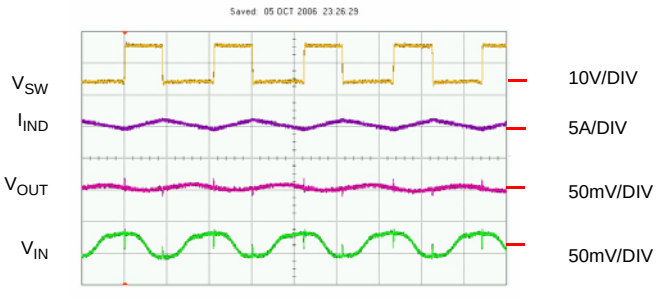
Figure 14: PWM Mode



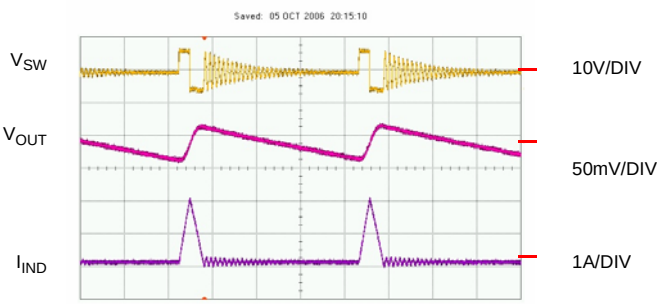
C_{IN} = **4x22µF**
V_{IN} = 12V
V_{OUT} = 5V
I_{LOAD} = 5A
$V_{OUT(P-P)}$ = 22.7mV (note)
$V_{IN(P-P)}$ = 57.1mV
$I_{IND(P-P)}$ = 2.1A
$I_{IND(PK)}$ = 6A
Frequency = 500kHz

Figure 15: PWM Mode



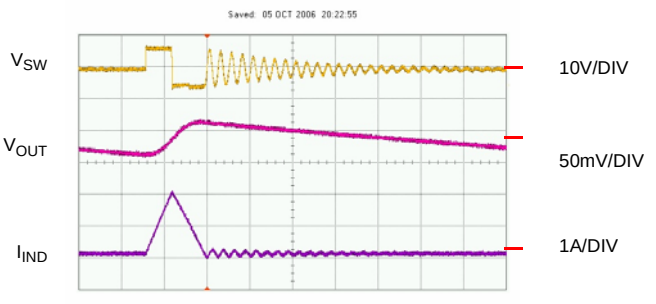
C_{IN} = **8x22µF**
V_{IN} = 12V
V_{OUT} = 5V
I_{LOAD} = 5A
$V_{OUT(P-P)}$ = 28.3mV (note)
$V_{IN(P-P)}$ = 47.6mV
$I_{IND(P-P)}$ = 2.06A
$I_{IND(PK)}$ = 6.05A
Frequency = 500kHz

Figure 16: DCM Mode



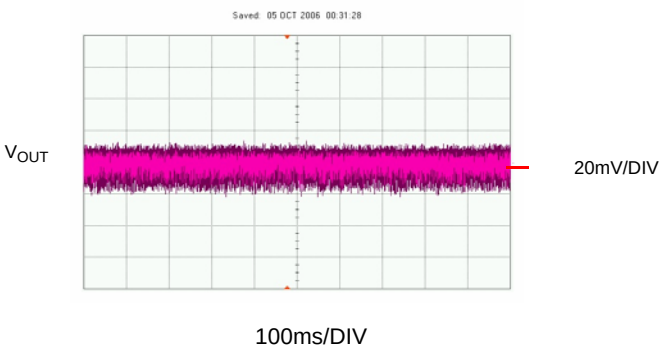
V_{IN} = 12V
V_{OUT} = 5V
$V_{OUT(P-P)}$ = 60.4mV (note)
I_{LOAD} = 24mA
$I_{IND(PK)}$ = 1.82A
Frequency = 49kHz

Figure 17: DCM Mode-zoom



V_{IN} = 12V
V_{OUT} = 5V
I_{LOAD} = 24mA
Ringing Frequency = 1.8MHz

Figure 18: PWM Output Ripple Voltage



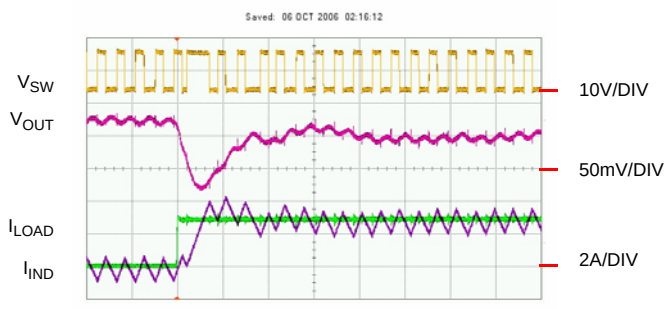
V_{IN} = 12V I_{LOAD} = 5A

V_{OUT} = 5V $V_{OUT(P-P)}$ = 35.3mV (Note)

4.3 Load Transient Waveforms

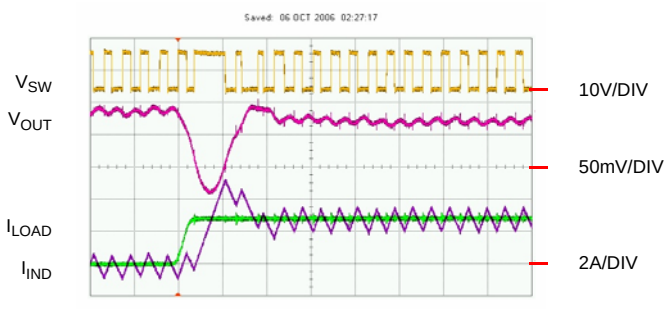
4.3.1 Step-Down Regulator

Figure 19: Fast Load Rise Time



V_{IN} = 12V
V_{OUT} = 5V
I_{LOAD} = 2A to 5A
C_{OUT} = **4 x 47µF**
t_{RISE} = 50A/µs

Figure 20: Slow Load Rise Time

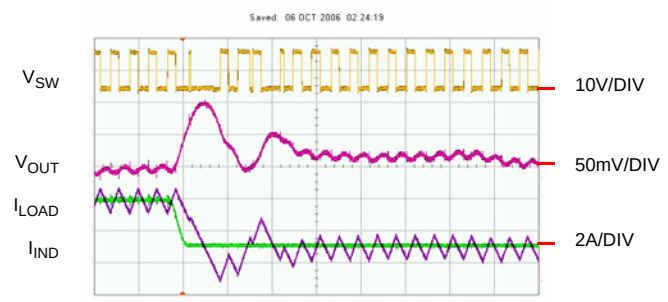


V_{IN} = 12V
V_{OUT} = 5V
I_{LOAD} = 2A to 5A
C_{OUT} = **4 x 47µF**
t_{RISE} = 2.5A/µs

Figure 21: Fast Load Fall Time

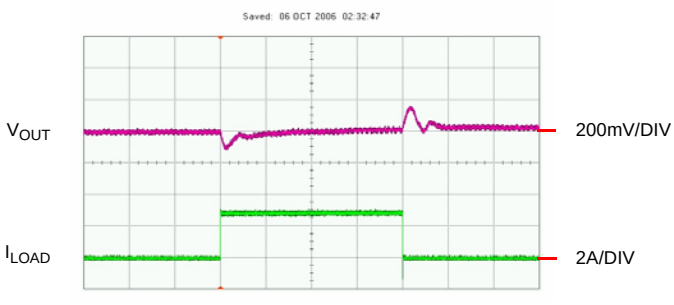
V_{IN} = 12V
V_{OUT} = 5V
I_{LOAD} = 5A to 2A
C_{OUT} = **4 x 47µF**
t_{RISE} = 230A/µs

Figure 22: Slow Load Fall Time



V_{IN} = 12V
V_{OUT} = 5V
I_{LOAD} = 5A to 2A
C_{OUT} = **4 x 47µF**
t_{RISE} = 2.5A/µs

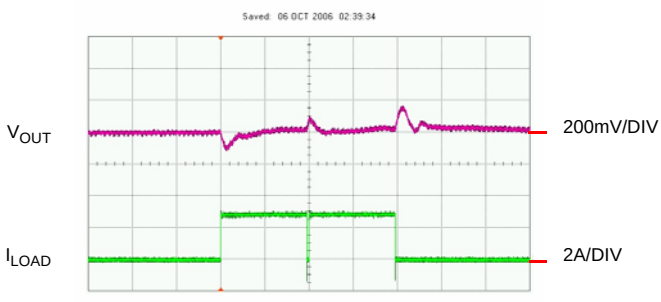
Figure 23: Load Transient Response



20µs/DIV

V_{IN} = 12V
V_{OUT} = 5V
I_{LOAD} = 2A to 5A
C_{OUT} = **4 x 47µF**
t_{RISE} = 50A/µs
t_{FALL} = 230A/µs

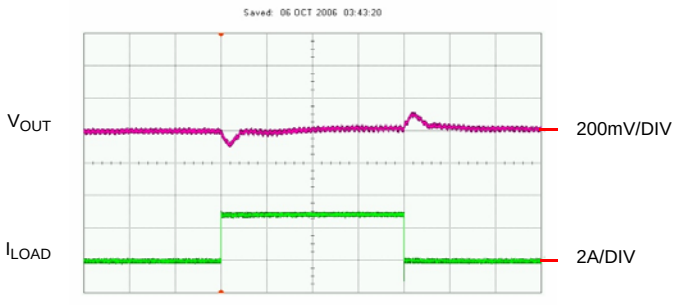
Figure 24: Double-Pulsed Load Response



20µs/DIV

V_{IN} = 12V
V_{OUT} = 5V
I_{LOAD} = 2A to 5A
C_{OUT} = **4 x 47µF**
t_{RISE} = 50A/µs
t_{FALL} = 230A/µs

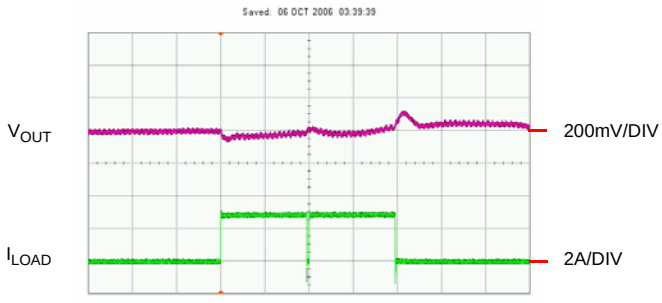
Figure 25: Load Transient Response



20µs/DIV

V_{IN} = 12V
V_{OUT} = 5V
I_{LOAD} = 1A to 3A
C_{OUT} = **4 x 47µF**
t_{RISE} = 50A/µs
t_{FALL} = 230A/µs

Figure 26: Double-Pulsed Load Response



20µs/DIV

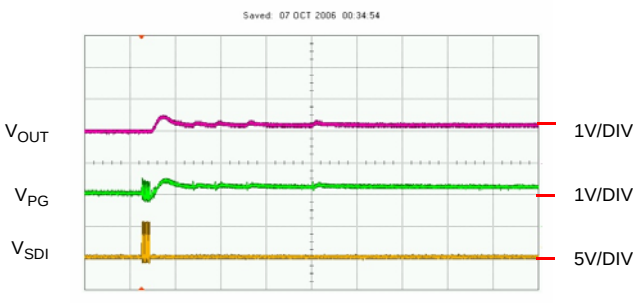
V_{IN} = 12V
V_{OUT} = 5V
I_{LOAD} = 1A to 3A
C_{OUT} = **4 x 47µF**
t_{RISE} = 50A/µs
t_{FALL} = 230A/µs

4.4 Output Voltage Transient Waveforms

The following graphs show the effect of changing the step-down regulator's output voltage using the serial interface. Depending on the change in the step-size of the output voltage, the output load, and the output capacitance, the power-on reset pin de-asserts when the changes of the output voltage occur beyond the 25µs (typical) delay.

4.4.1 Step-Down Regulator

Figure 27: V_{OUT} = 1.0V to 1.2V with I_{Load} = 0A

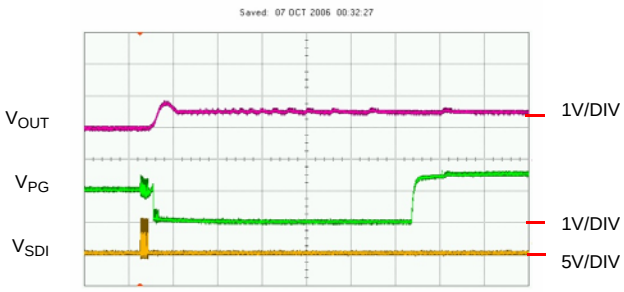


100µs/DIV

V_{IN} = 12V

C_{OUT} = (4 x 47µF) + 1000µF

Figure 28: V_{OUT} = 1.0V to 1.5V with I_{Load} = 0A



100µs/DIV

V_{IN} = 12V

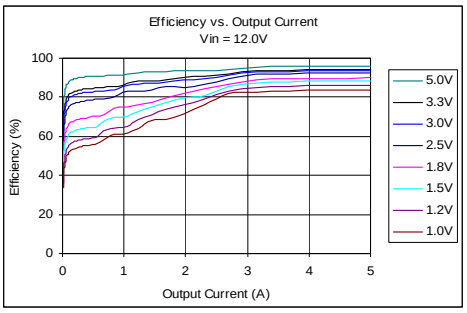
C_{OUT} = (4 x 47µF) +1000µF

5 Typical Characteristics

Unless otherwise noted, the following typical scope photographs were taken using test circuit shown in figure 1 at T_A = 25°C.

5.1 Efficiency

Figure 29: Efficiency vs. Output Current



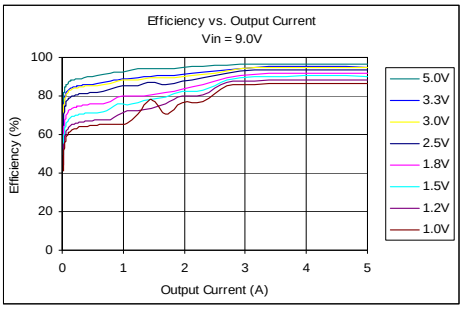
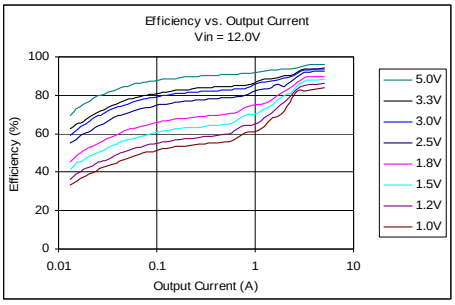
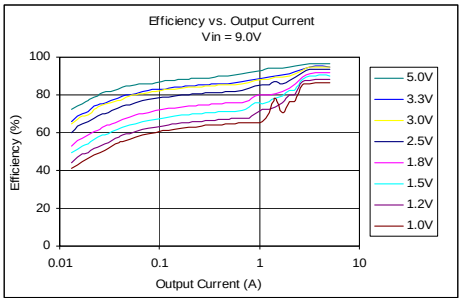


Figure 30: Efficiency vs. Output Current in Log Scale

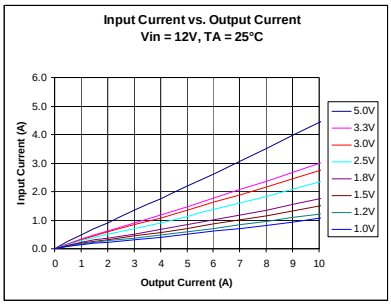




5.2 IC Case, MOSFET, and Inductor Temperature

The following data was taken using a 2.0 square inch PCB 1 oz. copper and L = 4.2µH. Actual results depend upon the size of the PCB proximity to other heat emitting components

Figure 31: Input Current vs. Output Current



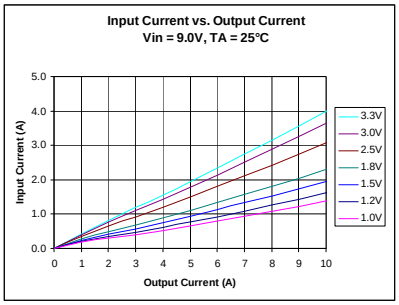
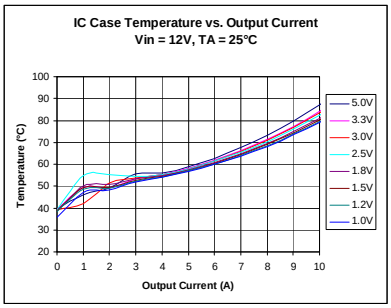


Figure 32: IC Case Temperature vs. Output Current



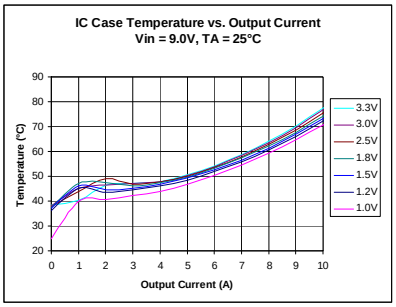
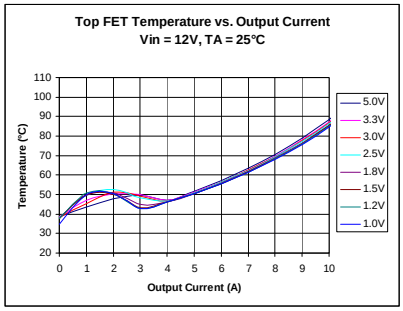


Figure 33: Top FET Temperature vs. Output Current



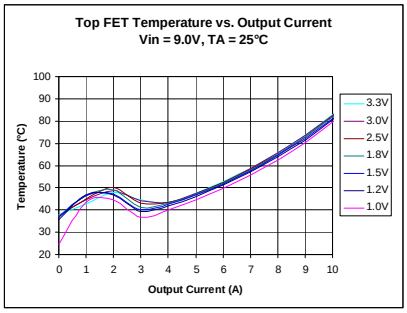
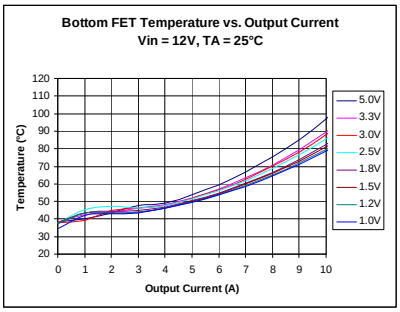


Figure 34: Bottom FET Temperature vs. Output Current



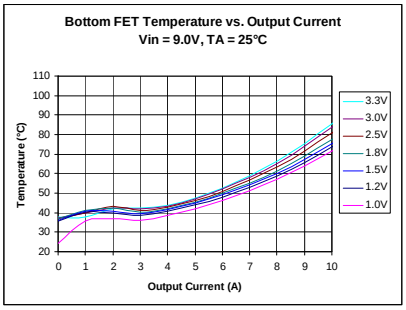
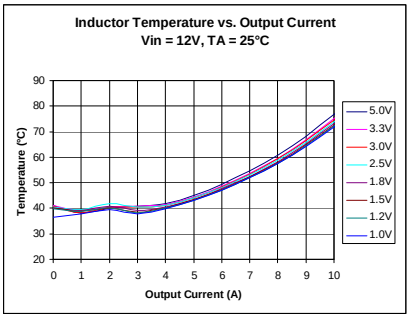
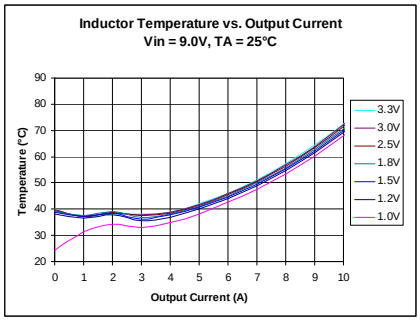


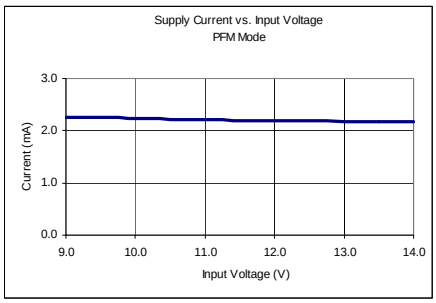
Figure 35: Inductor Temperature vs. Output Current





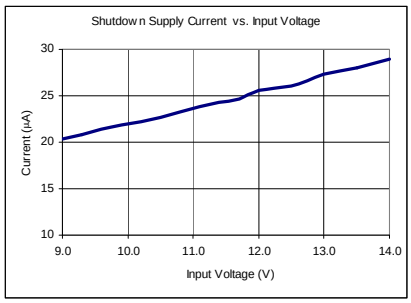
5.3 Input Voltage

Figure 36: Supply Current vs. Input Voltage



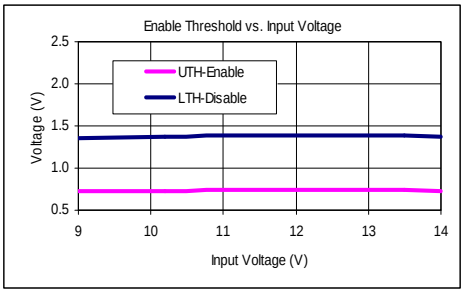
I_{LOAD} = No Load

Figure 37: Shutdown Supply Current vs. Input Voltage



V_{IN} = 12V; I_{LOAD} = No Load; V_{EN} = 0V

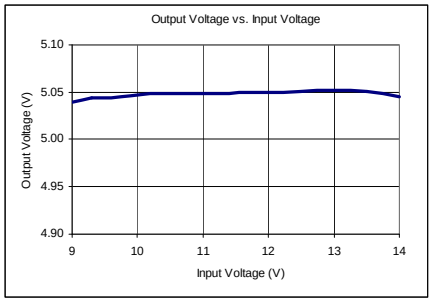
Figure 38: Enable Threshold vs. Input Voltage



I_{LOAD} = 10mA

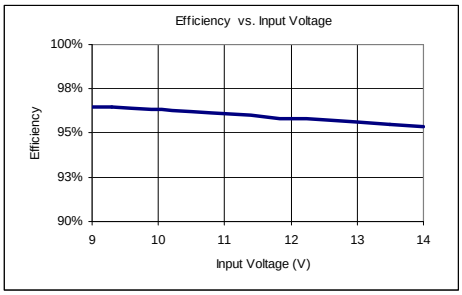
5.3.1 Step-down Regulator

Figure 39: Output Voltage vs. Input Voltage



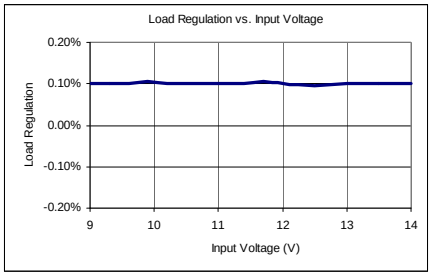
I_{LOAD} = 2.5A

Figure 40: Efficiency vs. Input Voltage



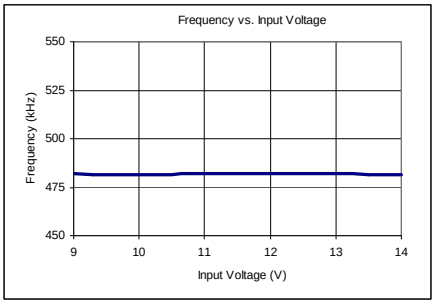
V_{OUT} = 5V; I_{LOAD} = 5A

Figure 41: Load Regulation vs. Input Voltage



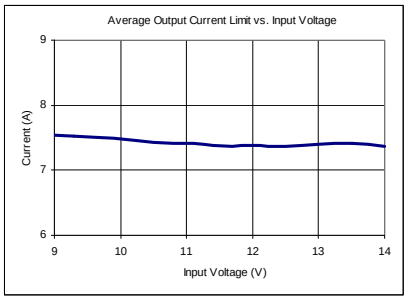
V_{OUT} = 5V; I_{LOAD} = 2.5 - 5A

Figure 42: Frequency vs. Input Voltage



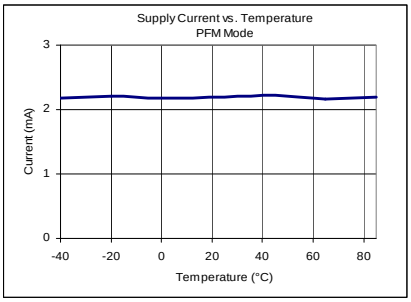
V_{OUT} = 5V; I_{LOAD} = 5A

Figure 43: Average Output Current Limit vs. Input Voltage



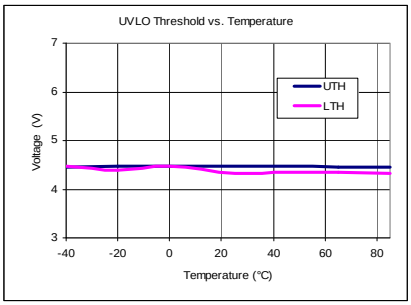
5.4 Temperature

Figure 44: Supply Current vs. Temperature



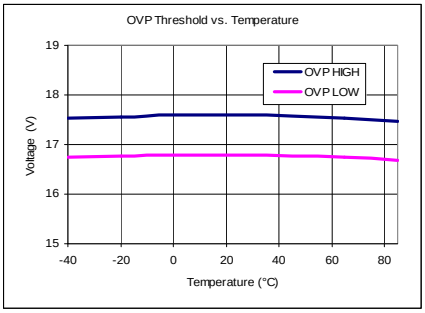
I_{LOAD} = No Load; V_{PWM} = 0V

Figure 45: UVLO Threshold vs. Temperature



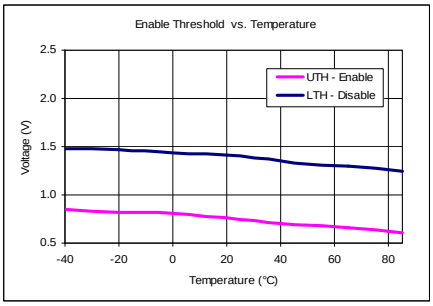
I_{LOAD} = 10mA

Figure 46: OVP Threshold vs. Temperature



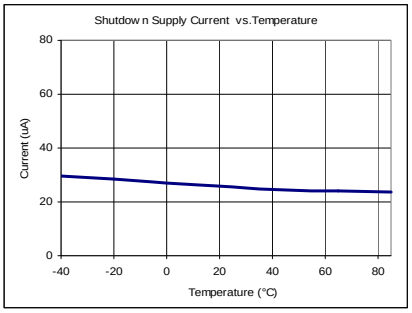
I_{LOAD} = 10mA

Figure 47: Enable Threshold vs. Temperature



I_{LOAD} = 10mA

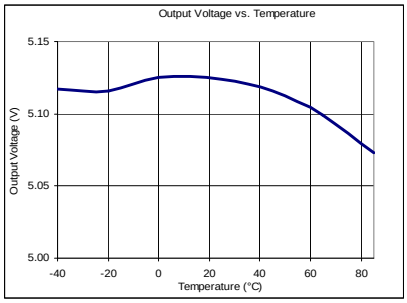
Figure 48: Shutdown Supply Current vs. Temperature



I_{LOAD} = No Load; V_{EN} = 0V

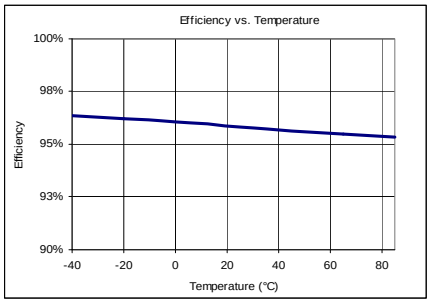
5.4.1 Step-down Regulator

Figure 49: Output Voltage vs. Temperature



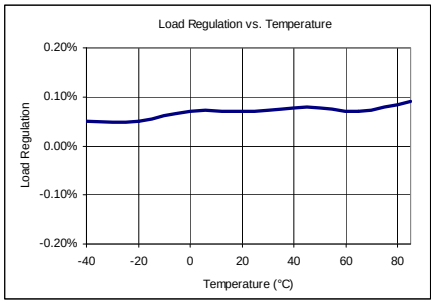
V_{IN} = 12V; I_{LOAD} = 2.5A

Figure 50: Efficiency vs. Temperature



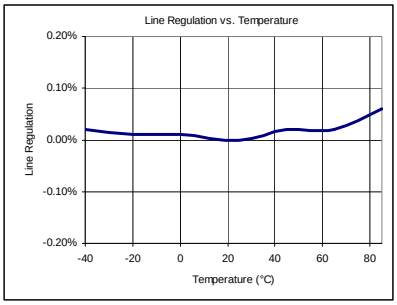
V_{IN} = 12V; V_{OUT} = 5V; I_{LOAD} = 5A

Figure 51: Load Regulation vs. Temperature



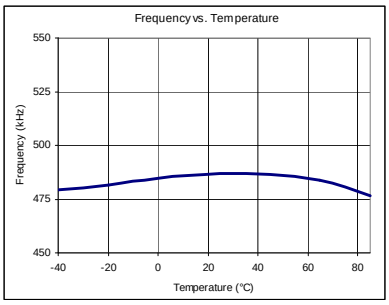
V_{IN} = 12V; V_{OUT} = 5V; I_{LOAD} = 2.5A - 5A

Figure 52: Line Regulation vs. Temperature



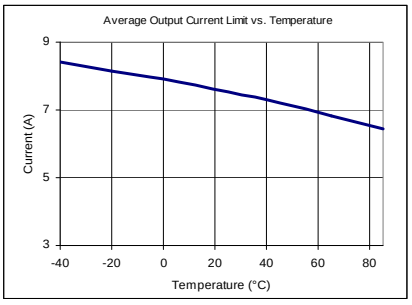
V_{IN} = 9V - 12V; V_{OUT} = 5V; I_{LOAD} = 5A

Figure 53: Frequency vs. Temperature



V_{IN} = 12V; I_{LOAD} = 5A

Figure 54: Average Output Current Limit vs. Temperature



V_{IN} = 12V

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6 Applications Information

6.1 PC Board Layout Considerations and Guidelines

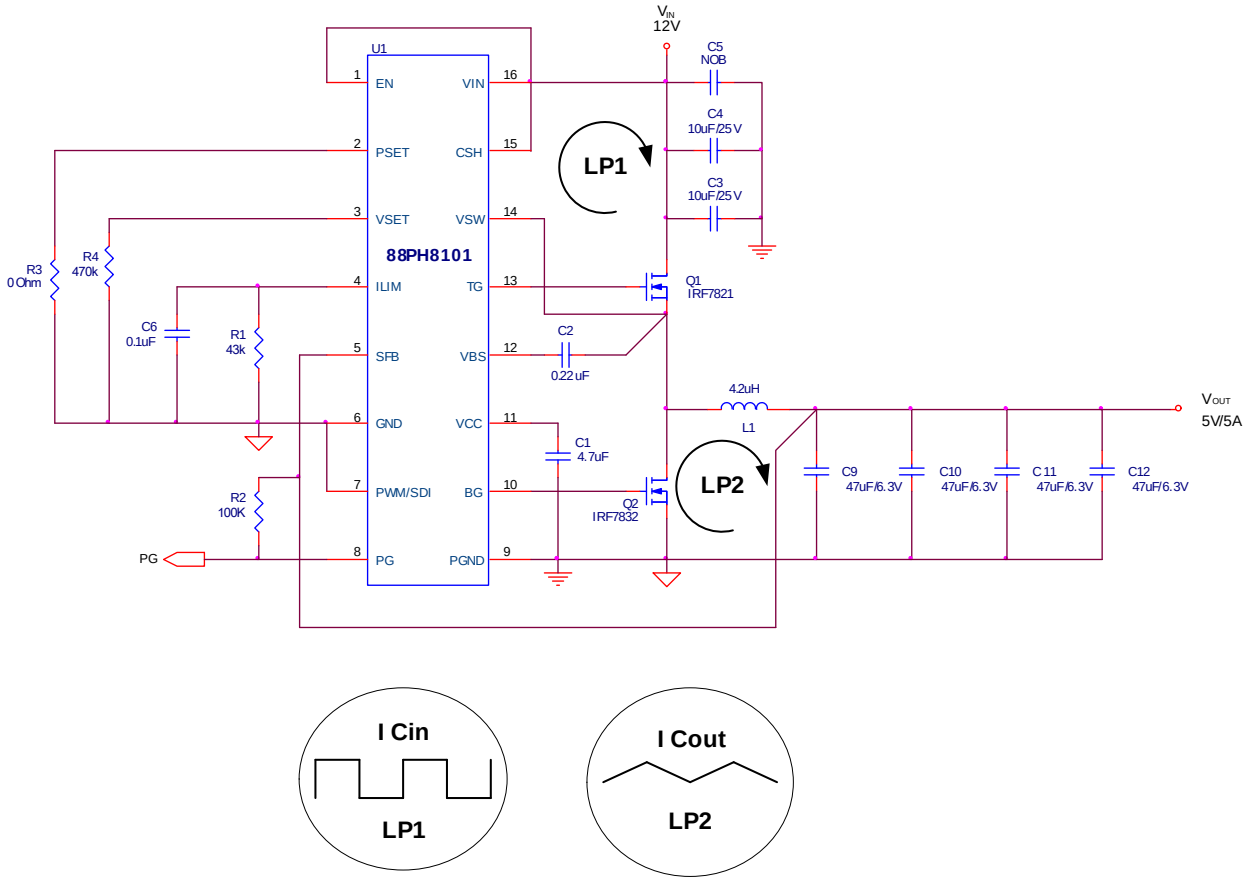
Warning	To avoid noise and abnormal operating behavior, follow these layout recommendations.

The PC board layout is very critical in any switching converter. An improper layout can contribute to system instability, excessive Electro-Magnetic Interference (EMI), and high switching loss. Follow these basic guidelines for good PC layout:

1. Copy the layout on page 47 as much as possible and use the recommend BOM on page 51. Contact the factory if substitutions are made.
2. Review the recommended solder pad layout and notes on page 53.
3. Do not replace the Ceramic input or output capacitors with Tantalum capacitors!
4. Any type of capacitor can be placed in parallel with the input capacitor as long as the Ceramic input capacitor is placed next to the IC. If Tantalum input capacitor is used, it must be rated for switching regulator applications and the operating voltage be derated by 50%.
5. Any type of capacitor can be placed in parallel with the output capacitor.
6. Low-ESR capacitors like the POSCAP from Sanyo can replace the Ceramic output capacitors as long as the capacitor value is the same or greater. Note that the Ceramic capacitors provide the lowest noise and smallest foot print solution.
7. Use planes for the ground, input and outputs power to maintain good voltage filtering and to keep power losses low.
8. If there is not enough space for a power plane for the input supply, then the input supply trace must be at least 3/8 inch wide.
9. If there is not enough space for a power plane for the output supplies, then place the output as close to the load as possible with a trace of at least 3/8 inch wide.
10. Do not lay out the inductor first. **The input capacitors, Q1 and Q2 placement are the most critical for proper operation.** These components must be placed as close as possible to each other with as short and wide trace as possible. The AC current circulating through these components and loop 1 (LP1) are square wave with rise and fall times of 8ns and slew rates as high as 300A/µs (see Figure 11). At these fast slew rates, stray PCB inductance can generate a voltage spike as high as 3V per inch of PCB trace, VIND = L * di/dt. Also, the VIN and PGND traces must be placed on the top layer. This will isolate the fast AC currents from interfering with the analog ground plane.
11. Place the bootstrap capacitor, C2, as close as possible to the VBS and VSW pins.
12. The 88PH8101 has two internal grounds, analog (GND) and power (PGND). The analog ground ties to all the noise sensitive signals (PSET, VSET, and VCC) while the power ground ties to the higher current power paths. Noise on an analog ground can cause problems with the IC's internal control and bias signals. For this reason, separate analog and power ground traces are recommended. The signal ground is connected to the power ground at one point, which is the (-) terminal of the output capacitor.
13. Connect the CSH and VSW pins as close to Q1 drain and source as possible. These pins are the sense terminals of the current limit comparator circuitry.

14. The VIN pin is sensitive to noise; therefore, connect the VIN pin to the (+) terminal of the input capacitor and distance the PVIN from the CSH connection as far as possible.
15. Connect the (-) terminal of the output capacitor as close to the (-) terminal of the input capacitor. A back-to-back placing of bypass capacitors, as shown in Figure 55, is recommended for best results.
16. Keep the switching node (VSW) away from the SFB pin and all sensitive signal nodes, minimizing capacitive coupling effects. If the SFB trace must cross the VSW node, cross it at a right angle.
17. Try not to route analog or digital lines in close proximity to the power supply especially the VSW node. If this can't be avoided, shield these lines with a power plane placed between the VSW node and the signal lines.

Figure 55: PCB Board Schematic



6.1.1 PC Board Layout Example

- Actual board size = 1450 mil x 1330 mil
- Total copper layers = 4
- All the components are on the top layer

Figure 56: Top Silk-Screen, Top Traces, Vias, and Copper (Not to Scale)

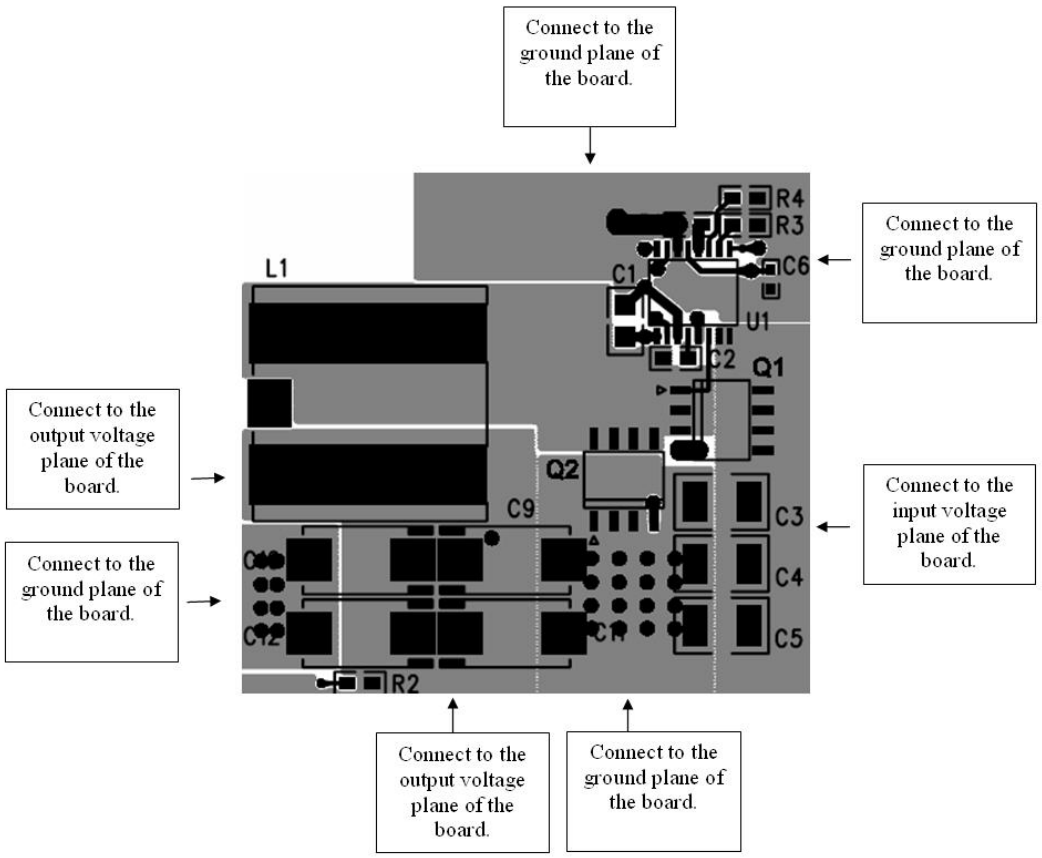


Figure 57: GND_Layer2 Vias, and Copper (Not to Scale)

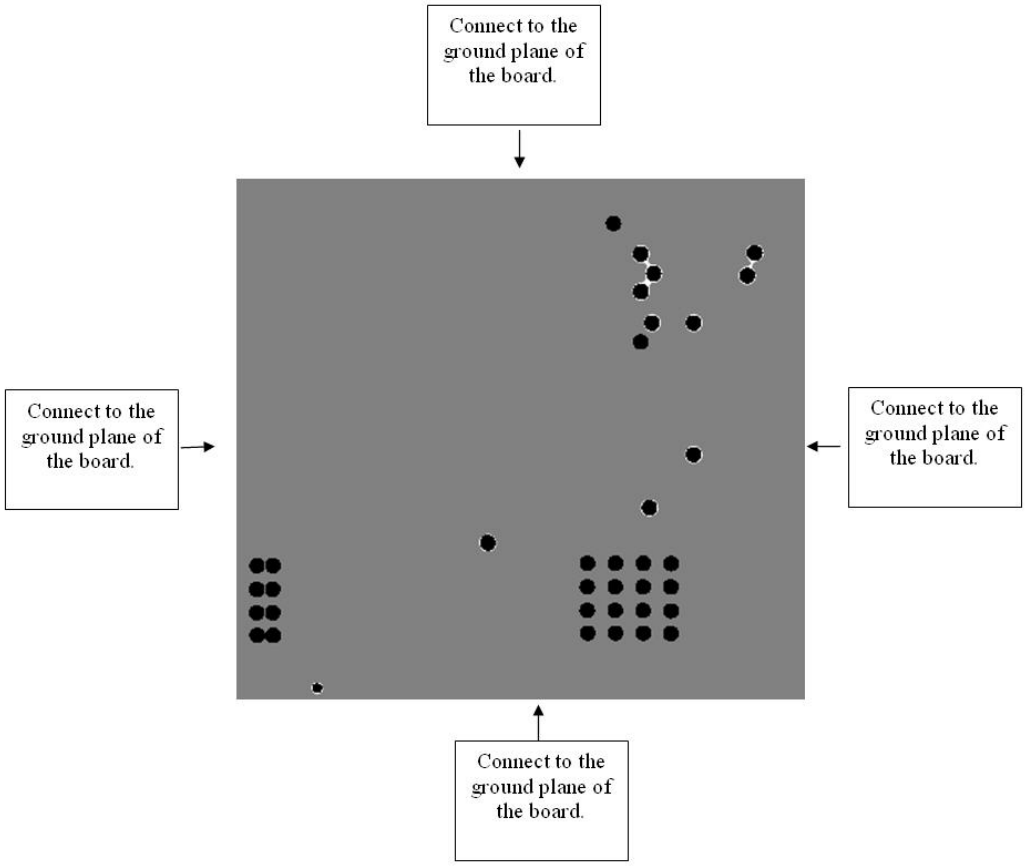


Figure 58: GND_Layer3 Vias, and Copper (Not to Scale)

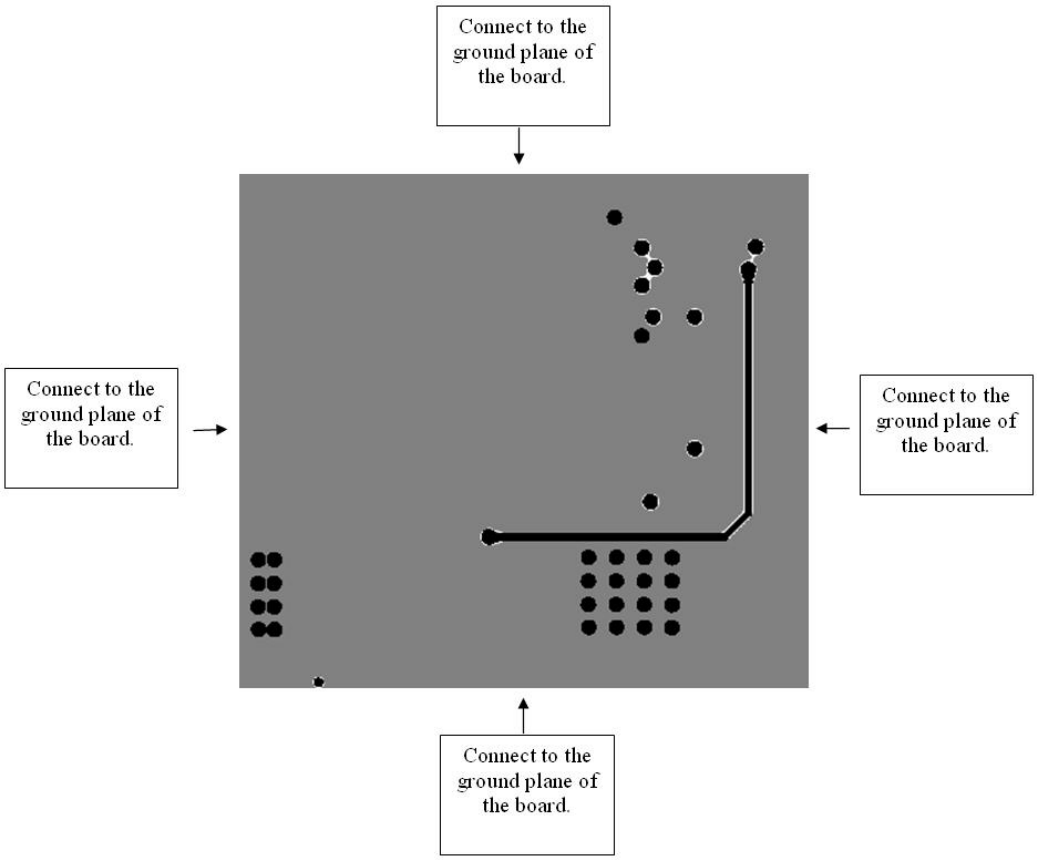
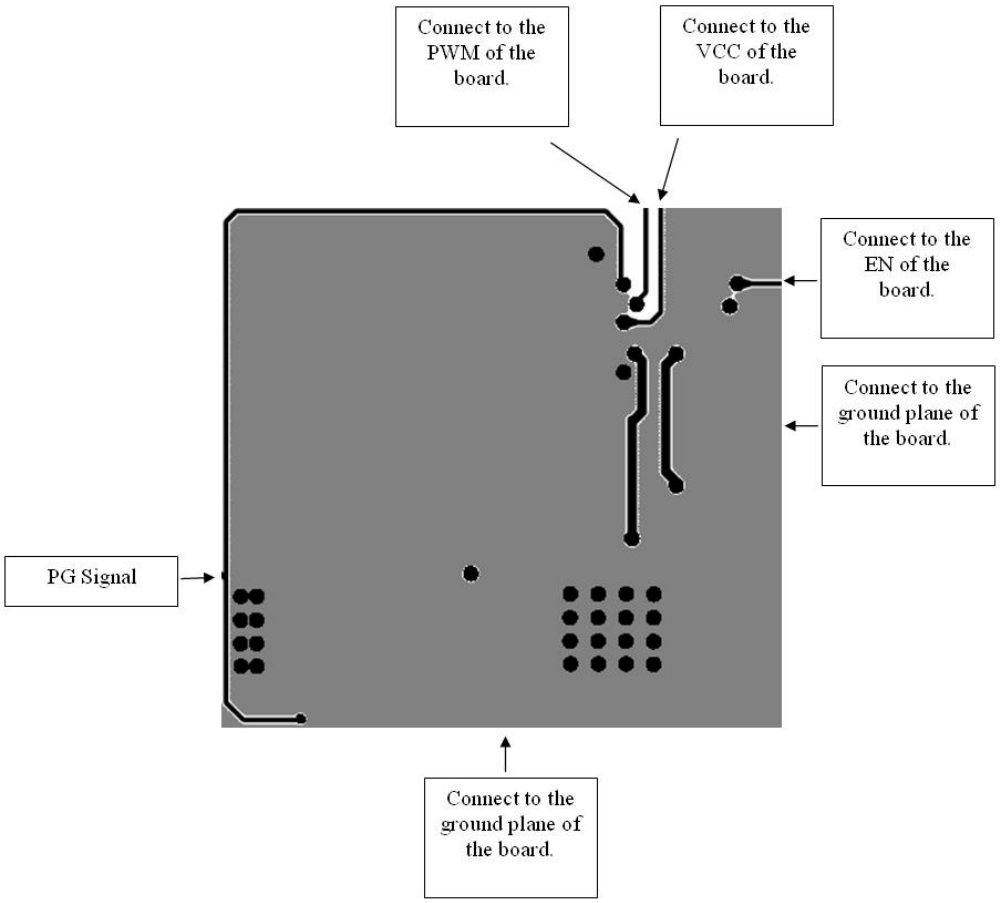


Figure 59: Bottom Silk Screen, Bottom Traces, Vias, and Copper (Not to Scale)



6.1.2 Bill of Materials

Table 12: BOM

Item	Qty	Ref	Manufacturer	Manufacturer Part No.	Description
1	**1**	**U1**	**Marvell Semiconductor**	**88PH8101**	**High Voltage Switching Regulator Controller**
2	1	C1	Murata	GRM21BR71C475K	CAP CER 4.7µF 16V 10% X7R 0805
3	1	C2	Murata	GRM188R61A224KA01D	CAP CER 0.22µF 10V 10% X5R 0603
4	1	C3	Murata	GRM32DR61E106KA12L	CAP CER 10µF 25V 10% X5R 1210
5	1	C4	Murata	GRM32DR61E106KA12L	CAP CER 10µF 25V 10% X5R 1210
6	0	C5	--	NOB	NOT ON BOARD
7	1	C6	TDK Corporation	C1608X7R1E104K	CAP CER 0.1µF 25V X7R 10% 0603
8	1	C9	TDK Corporation	C3216X5R0J476M	CAP CER 47µF 6.3V X5R 20% 1206
9	1	C10	TDK Corporation	C3216X5R0J476M	CAP CER 47µF 6.3V X5R 20% 1206
10	1	C11	TDK Corporation	C3216X5R0J476M	CAP CER 47µF 6.3V X5R 20% 1206
11	1	C12	TDK Corporation	C3216X5R0J476M	CAP CER 47µF 6.3V X5R 20% 1206
12	1	L1	Sumida	CDEP145NP-4R2MC-170	CDEP145 Series, 4.2µH, 12.3A @ 20°C, 7.4 mΩ, H = 6 mm, L = 14.9 mm, W = 14.9 mm
13	1	Q1	IRF	IRF7821TRPBF	N-Channel MOSFETs SO-8 30V 13.6A @ 25°C
14	1	Q2	IRF	IRF7832PBFCT	N-Channel MOSFETs SO-8 30V 20A
15	1	R1	Yageo Corporation	RC0603JR-0743KL	RES 43KΩ 1/10W 5% 0603 SMD
16	1	R2	Panasonic - ECG	ERJ-3GEYJ104V	RES 100KΩ 1/10W 5% 0603 SMD
17	1	R3	Yageo America	RC0603JR-070RL	RES 0.0Ω 1/10W 5% 0603 SMD
18	1	R4	Yageo Corporation	RC0603JR-07470KL	RES 470KΩ 1/10W 5% 0603 SMD

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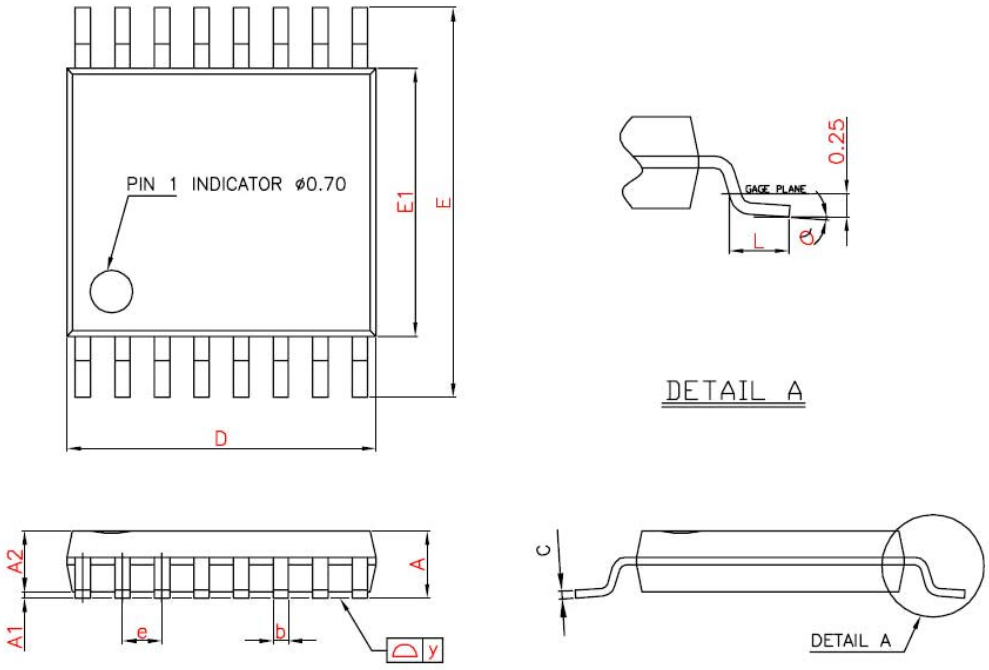
7 Mechanical Drawings

7.1 Mechanical Drawing

Figure 60: 16-Pin TSSOP Mechanical Drawing



7.2 Mechanical Dimensions

Table 13: 16-Pin TSSOP Dimensions

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.05	1.10	1.20	0.041	0.043	0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2		1.00	1.05		0.039	0.041
b	0.20	0.25	0.28	0.008	0.010	0.011
C		0.127			0.005	
D	4.90	5.00	5.10	0.193	0.200	0.200
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.170	0.173	0.177
e		0.65			0.026	
L	0.50	0.60	0.70	0.020	0.024	0.028
y			0.076			0.003
α	0°	4°	8°	0°	4°	8°

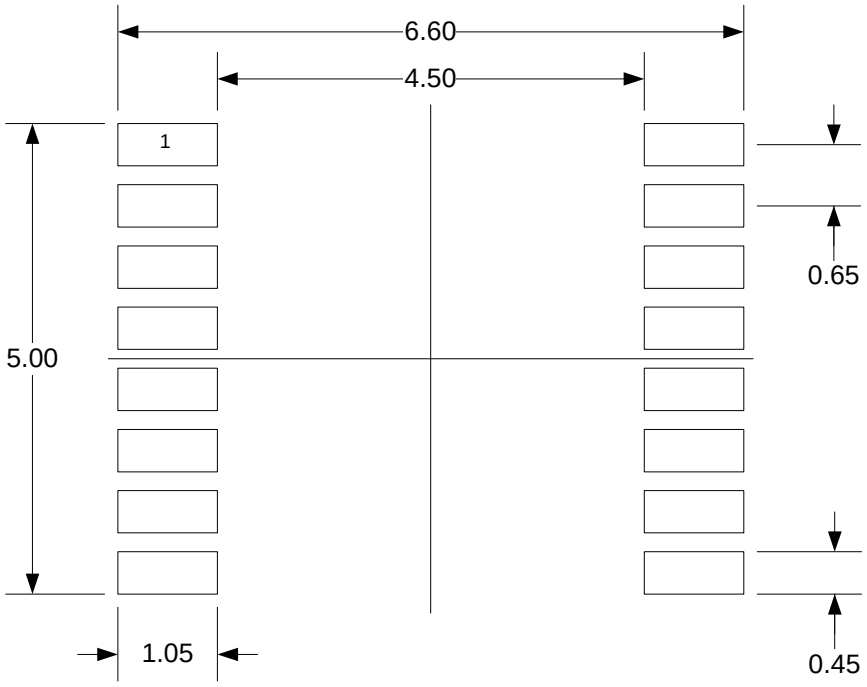
Notes:

1. CONTROLLING DIMENSION: mm
2. DIMENSION “D” DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MODE FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006” [0.15mm] PER END DIMENSION “E1” DOES NOT INCLUDE INTERLEAD FLASH INTERLEAD FLASH SHALL NOT EXCEED 0.010” [0.25mm] PER SIDE.
3. REFERENCE DOCUMENT: JEDEC SPEC MO-153

7.3 Typical Pad Layout Dimensions

7.3.1 Recommended Solder Pad Layout

Figure 61: TSSOP-16 Land Pattern (mm)



Notes:

1. TOP VIEW
2. DRAWING NOT TO SCALE
3. CONTROLLING DIMENSION: mm
4. OVERSIZE SOLDER MASK BY 4 MILS OVER PAD SIZE (2 MIL ANNULAR RING)
5. TOLERANCE ±0.05mm

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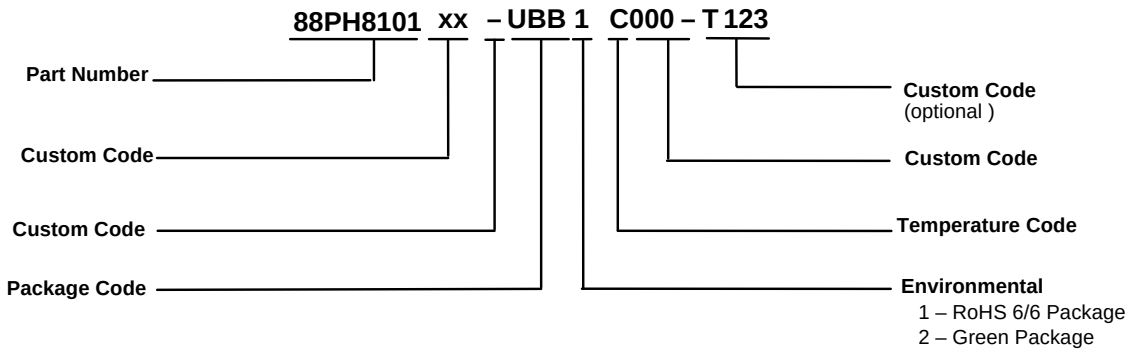
8 Part Order Numbering / Package Marking

8.1 Part Order Numbering Scheme

Figure 62 shows the part order numbering scheme. Refer to a Marvell® Field Application Engineer (FAE) or sales representative for further information when ordering parts.

Figure 62: Sample Part Number



8.2 Part Ordering Options

The standard ordering part numbers for the respective solutions are as follows:

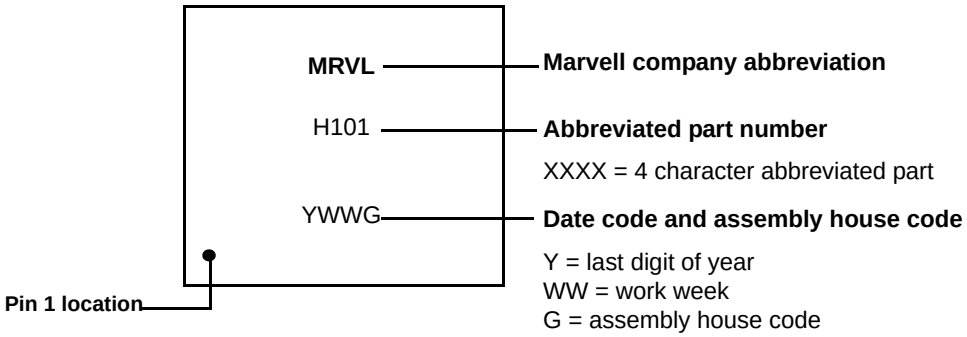
Table 14: Part Ordering Options

Package Type	Part Order (booking) Number
16-pin TSSOP	88PH8101xx-UBB1C000
16-pin TSSOP	88PH8101xx-UBB1C000-T (Tape and Reel)

8.3 Package Marking

Figure 63 shows a sample package marking and pin 1 location.

Figure 63: Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings are approximate.

A Revision History

Table 15: Revision History

Document Type	Document Revision
Release	Rev. –
Updated to new template, Removed all “88PH8201” instances, Removed “Confidential”, Updated Typ. Dwg. (Fig. 1), Updated Electrical Chars. Output Voltage Specs., Updated Logic Programmability Voltage Output Specs. (Table 3), Replaced PC Board Schematic, Replaced and added silk screens (Fig. 30 - Fig. 34), Updated Bill of Materials.	

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