Device Features

BlueCore™4-ROM

- Fully Qualified Bluetooth v2.1 + EDR system
- Enhanced Data Rate (EDR) compliant with v2.1 of specification for both 2Mbps and 3Mbps modulation modes
- Full Speed Bluetooth Operation with Full Piconet Support
- Scatternet Support
- Low power 1.8V operation
- Small footprint 6 x 6mm 84-ball VFBGA Package
- Minimum External Components Required
- Integrated 1.8V Regulator
- USB and Dual UART Ports to 3Mbits/s
- Support for 802.11 (Wi-Fi) Coexistence
- RoHS Compliant

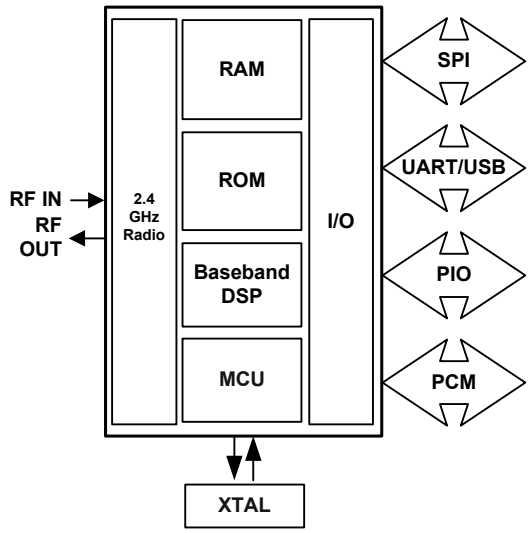
Single Chip Bluetooth®
v2.1 + EDR System

Production Data Sheet For
BC41B143A07
November 2007

General Description

BlueCore™4-ROM is a single-chip radio and baseband IC for Bluetooth 2.4GHz systems including enhanced data rates (EDR) to 3Mbps.

With the on-chip CSR Bluetooth software stack it provides a fully compliant Bluetooth system to v2.1 of the specification for data and voice communications.



System Architecture

Applications

- MP3 Players
- Portable Media Players
- Internet Radios
- Hi-Fi Systems
- Digital cameras and other high volume consumer products

BlueCore4-ROM is designed to reduce the number of external components required. This ensures that production costs are minimised.

The device incorporates auto-calibration and *built in self test* (BIST) routines to simplify development, type approval and production test. All hardware and device firmware is fully compliant with the Bluetooth v2.1 + EDR Specification (all mandatory features).

BlueCore™4-ROM Product Data Sheet

Contents

Status Information

The status of this Data Sheet is **Production Information**.

CSR Product Data Sheets progress according to the following format:

Advance Information

Information for designers concerning CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

Pre-Production Information

Pinout and mechanical dimension specifications finalised. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All electrical specifications may be changed by CSR without notice.

Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

Production Data Sheets supersede all previous document versions.

Life Support Policy and Use in Safety-Critical Applications

CSR's products are not authorised for use in life-support or safety-critical applications. Use in such applications is done at the sole discretion of the customer. CSR will not warrant the use of its devices in such applications.

RoHS Compliance

BlueCore4-ROM devices meet the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS).

Trademarks, Patents and Licenses

Unless otherwise stated, words and logos marked with ™ or ® are trademarks registered or owned by CSR plc or its affiliates. Bluetooth® and the Bluetooth logos are trademarks owned by Bluetooth SIG, Inc. and licensed to CSR. Other products, services and names used in this document may have been trademarked by their respective owners.

The publication of this information does not imply that any license is granted under any patent or other rights owned by CSR plc.

CSR reserves the right to make technical changes to its products as part of its development programme.

While every care has been taken to ensure the accuracy of the contents of this document, CSR cannot accept responsibility for any errors.

1 Key Features

Radio

- Common TX/RX terminals simplify external matching and eliminates external antenna switch
- BIST minimises production test time. No external trimming is required in production
- Full RF reference designs are available
- Bluetooth v2.1+EDR Specification compliant

Transmitter

- +6dBm RF transmit power with level control from on-chip 6-bit DAC over a dynamic range >30dB
- Class 2 and Class 3 support without the need for an external power amplifier or TX/RX switch
- Class1 support using external power amplifier with RF power controlled by an internal 8-bit DAC
- Supports DQPSK (2Mbps) and 8DPSK (3Mbps) modulation

Receiver

- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real-time digitised RSSI available on HCI interface
- Fast AGC for enhanced dynamic range
- Supports DQPSK and 8DPSK modulation
- Channel classification

Synthesiser

- Fully integrated synthesiser requires no external VCO, varactor diode, resonator or loop filter
- Compatible with an external crystal or with an external clock using sinusoidal or logic-level signals
- Accepts frequencies between 8 and 32MHz (in multiples of 250kHz); additionally accepts 7.68, 14.4, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz TCXO frequencies typically used in GSM and CDMA devices

Auxiliary Features

- Crystal oscillator with built-in digital trimming
- Power management includes digital shutdown, and wake up commands with an integrated low-power oscillator for ultra low Park/Sniff/Hold mode
- Clock request output to control external clock

Auxilliary Features (Continued)

- On-chip linear regulator; 1.8V output from a 2.2 - 4.2V input
- Clock for low power mode can be either supplied from an external 32kHz clock signal or an internal oscillator
- Auto Data Rate setting for different TCXO frequencies
- Power-on-reset cell detects low supply voltage
- Aribitrary power supply sequencing permitted
- 8-bit ADC and DAC available to applications

Baseband and Software

- Internal 48-Kbyte RAM, allows full-speed data transfer, mixed voice and data, and full piconet operation, including all medium rate preset types
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping. Supports all Bluetooth v2.1 + EDR features including eSCO and AFH
- Transcoders for A-law, μ-law and linear voice from host and A-law, μ-law and CVSD voice over air

Physical Interfaces

- Synchronous serial interface up to 4Mbits/s for system debugging
- UART interface with programmable baud rate up to 3Mbits/s with an optional bypass mode
- Full-speed USB v2.0 interface supports OHCI and UHCI host interfaces
- Synchronous bi-directional serial programmable audio interface
- Optional I²C™ compatible interfaces
- Audio PCM interface
- Optional coexistence interfaces

Bluetooth Stack

CSR's Bluetooth Protocol Stack runs on the on-chip MCU in a variety of configurations:

- Standard HCI (UART or USB)
- Fully embedded RFCOMM
- Customised builds with embedded application code

Package Options

- 84-ball VFBGA 6.0 x 6.0 x 1.0mm, 0.5mm pitch

2 Package Information

2.1 BlueCore4-ROM Pinout Diagram

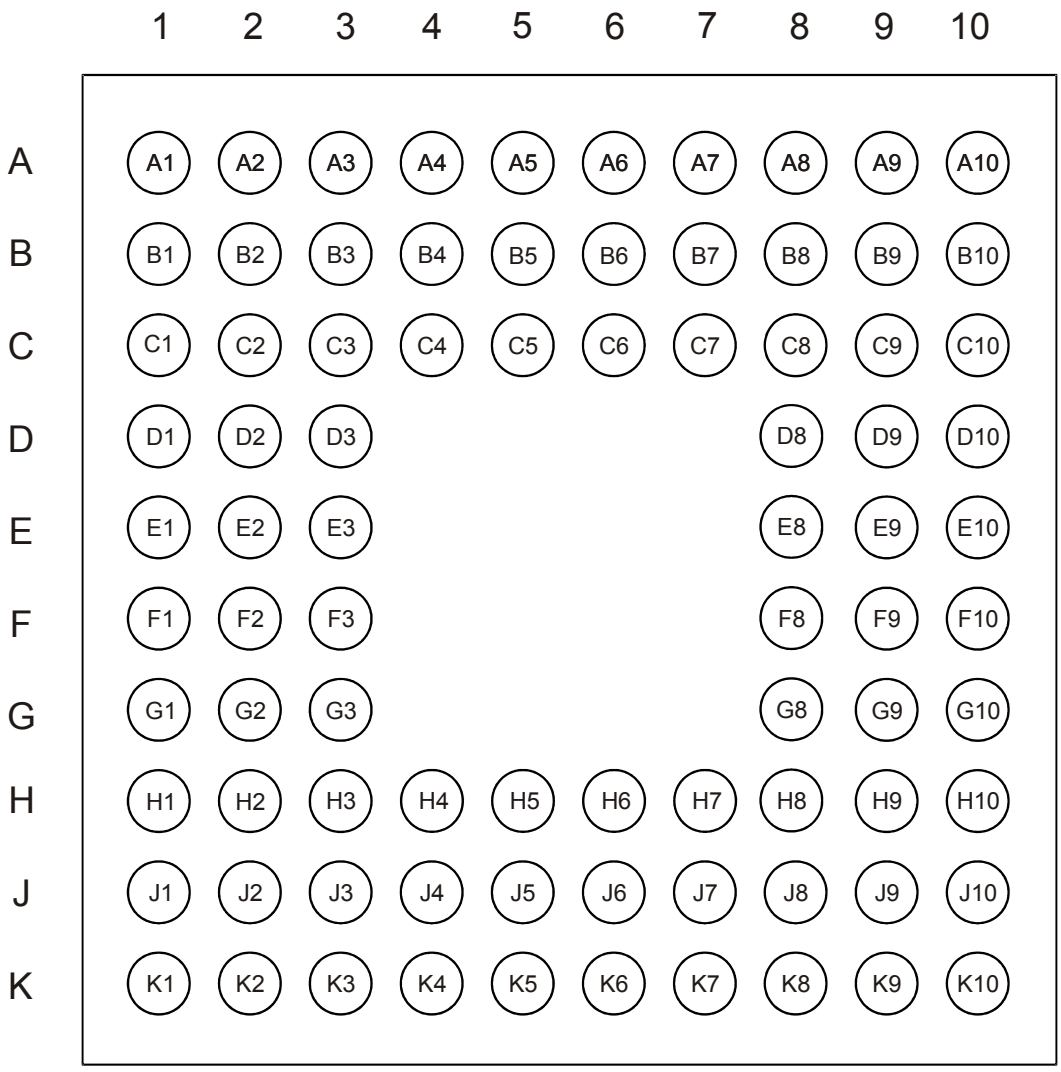


Figure 2.1: BlueCore4-ROM Device Pinout

2.2 Device Terminal Functions

Radio	Ball	Pad Type	Description
RF_IN	D1	Analogue	Single ended receiver input
PIO[0]/RXEN	B1	Bi-directional with programmable strength internal pull-up/down	Control output for external LNA (if fitted)
PIO[1]/TXEN	B2	Bi-directional with programmable strength internal pull-up/down	Control output for external PA (If fitted)
TX_A	F1	Analogue	Transmitter output/switched receiver input
TX_B	E1	Analogue	Complement of TX_A
AUX_DAC	D3	Analogue	Voltage DAC output

Synthesiser and Oscillator	Ball	Pad Type	Description
XTAL_IN	K3	Analogue	For crystal or external clock input
XTAL_OUT	J3	Analogue	Drive for crystal

USB and UART	Ball	Pad Type	Description
UART_TX	J10	CMOS output, tri-state, with weak internal pull-up	UART data output active high
UART_RX	H9	CMOS input with weak internal pull-down	UART data input active high
UART_RTS	H7	CMOS output, tri-state, with weak internal pull-up	UART request to send active low
UART_CTS	H8	CMOS input with weak internal pull-down	UART clear to send active low
USB_DP	J8	Bi-directional	USB data plus with selectable internal 1.5kΩ pull-up resistor
USB_DN	K8	Bi-directional	USB data minus

PCM Interface	Ball	Pad Type	Description
PCM_OUT	G8	CMOS output, tri-state, with weak internal pull-down	Synchronous data output
PCM_IN	G9	CMOS input, with weak internal pull-down	Synchronous data input
PCM_SYNC	G10	Bi-directional with weak internal pull-down	Synchronous data sync
PCM_CLK	H10	Bi-directional with weak internal pull-down	Synchronous data clock

Test and Debug	Ball	Pad Type	Description
RESET	C7	CMOS input with weak internal pull-down	Reset if high. Input debounced so must be low for >5ms to cause a reset
RESETB	D8	CMOS input with weak internal pull-up	Reset if low. Input debounced so must be low for >5ms to cause a reset
SPI_CSB	C9	CMOS input with weak internal pull-up	Chip select for Synchronous Serial Interface active low
SPI_CLK	C10	CMOS input with weak internal pull-down	Serial Peripheral Interface clock
SPI_MOSI	C8	CMOS input with weak internal pull-down	Serial Peripheral Interface data input
SPI_MISO	B9	CMOS output, tri-state, with weak internal pull-down	Serial Peripheral Interface data output
TEST_EN	C6	CMOS input with strong internal pull-down	For test purposes only (leave unconnected)

PIO Port	Ball	Pad Type	Description
PIO[11]	E3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[10]	C4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[9]	C3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line. Optional WLAN_ACTIVE for 3-wire 802.11 (Wi-Fi) co-existence signalling (a)
PIO[8]	C5	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[7]	F9	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line. RF_ACTIVE for 3-wire 802.11 (Wi-Fi) co-existence signalling
PIO[6]	F10	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line. Optional WLAN_ACTIVE for 2-wire 802.11 (Wi-Fi) co-existence signalling(a)
PIO[5]	F8	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line. BT_STATUS for 3-wire 802.11 (Wi-Fi) co-existence signalling
PIO[4]	E8	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line. Optional BT_PRIORITY for 2-wire 802.11 (Wi-Fi) co-existence signalling (a)
PIO[3]	B4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[2]	B3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
AIO[2]	J5	Bi-directional	Programmable input/output line
AIO[1]	H5	Bi-directional	Programmable input/output line
AIO[0]	H4	Bi-directional	Programmable input/output line

(a) Functionality defined as 'optional' can be assigned to another PIO using CSR's PS Keys.

Power Supplies and Control	Ball	Pad Type	Description
VREG_IN	K6	Linear regulator input	Linear regulator voltage input(a)
VREG_EN	K5	Input	High or not connected to enable regulator. VSS to disable regulator(a)
VDD_USB	K9	VDD	Positive supply for UART/USB ports and AIO ports
VDD_PIO	A3	VDD	Positive supply for PIO and AUX DAC(b)
VDD_PADS	D10	VDD	Positive supply for all other digital Input/Output ports(c)
VDD_CORE	E10	VDD	Positive supply for internal digital circuitry
VDD_RADIO	C1, C2	VDD	Positive supply for RF circuitry
VDD_VCO	H1	VDD	Positive supply for VCO and synthesiser circuitry
VDD_ANA	K4	VDD/Linear regulator output	Positive supply for analogue circuitry and 1.8V regulated output
VSS_PADS	A1, A2, D9, J9, K10	VSS	Ground connections for input/output
VSS_CORE	E9	VSS	Ground connection for internal digital circuitry
VSS_RADIO	D2, E2, F2	VSS	Ground connections for RF circuitry
VSS_VCO	G1, G2	VSS	Ground connections for VCO and synthesiser
VSS_ANA	J2, J4, K2	VSS	Ground connections for analogue circuitry
VSS	F3	VSS	Ground connection for internal package shield

(a) To enable the regulator the VREG_EN pin needs to be either pulled high or left unconnected. This preserves compatibility with BlueCore2-ROM since the corresponding pin on BlueCore2-ROM was designated a not connect pin. In BlueCore4-ROM the regulator is permanently on, replicating BlueCore2-ROM that has no regulator enable pin.

(b) Positive supply for PIO[3:0] and PIO[11:8]

(c) Positive supply for SPI/PCM ports and PIO[7:4]

Unconnected Terminals	Ball	Description
N/C	A4, A5, A6, A7, A8, A9, A10, B5, B6, B7, B8, B10, G3, H2, H3, H6, J1, J6, J7, K1, K7	Leave unconnected

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Rating	Min	Max
Storage Temperature	-40°C	+150°C
Supply Voltage: VDD_RADIO, VDD_LO, VDD_ANA and VDD_CORE	-0.4V	2.2V
Supply Voltage: VDD_PADS, VDD_PIO and VDD_USB	-0.4V	3.7V
Supply Voltage: VREG_IN	-0.4V	5.6V
Other Terminal Voltages	VSS-0.4V	VDD+0.4V

3.2 Recommended Operating Conditions

Operating Condition	Min	Max
Operating Temperature Range	-40°C	+105°C
Guaranteed RF performance range (a)	-40°C	+105°C
Supply Voltage: VDD_RADIO, VDD_LO, VDD_ANA and VDD_CORE	1.7V	1.9V
Supply Voltage: VDD_PADS, VDD_PIO and VDD_USB	1.7V	3.6V
Supply Voltage: VREG_IN	2.2V	4.2V(b)

(a) Typical figures are given for RF performance between -40°C and +105°C

(b) The device will operate without damage with VREG_IN as high as 5.6V, however the RF performance is not guaranteed above 4.2V

3.3 Linear Regulator

Linear Regulator	Min	Typ	Max	Unit
Normal Operation				
Output voltage (I_{load} = 70 mA / VREG_IN = 3.0V))	1.70	1.78	1.85	V
Temperature coefficient	-250	-	250	ppm/°C
Output noise[a] [b]	-	-	1	mV rms
Load regulation (I_{load} < 70 mA)	-	-	50	mV/A
Settling Time[a] [c]	-	-	50	µs
Maximum output current	70	-	-	mA
Minimum load current	5	-	-	µA
Input voltage	-	-	4.2[d]	V
Dropout voltage (I_{load} = 70 mA)	-	-	350	mV
Quiescent current (excluding load, I_{load} < 1mA)	25	35	50	µA
Low Power Mode[e]				
Quiescent current (excluding load, I_{load} < 100µA)	4	7	10	µA
Disabled Mode[f]				
Quiescent Current	1.5	2.5	3.5	µA

(a) Regulator output connected to 47nF pure and 4.7µF 2.2Ω ESR capacitors
(b) Frequency range is 100Hz to 100kHz
(c) 1mA to 70mA pulsed load
(d) Operation up to 5.6V is permissible without damage and without the output voltage rising sufficiently to damage the rest of BlueCore4-ROM, but output regulation and other specifications are no longer guaranteed at input voltages in excess of 4.2V
(e) Low power mode is entered and exited automatically when the chip enters/leaves Deep Sleep mode
(f) Regulator is disabled when VREG_IN is either open circuit or driven to the same voltage as VDD_ANA

3.4 Digital Terminals

Digital Terminals		Min	Typ	Max	Unit
Input Voltage Levels					
V_{IL} input logic level low	2.7V ≤ VDD ≤ 3.0V	-0.4	-	+0.8	V
	1.7V ≤ VDD ≤ 1.9V	-0.4	-	+0.4	V
V_{IH} input logic level high		0.7VDD	-	VDD+0.4	V
Output Voltage Levels					
V_{OL} output logic level low, (I_o = 4.0mA)[a] , 2.7V ≤ VDD ≤ 3.0V		-	-	0.2	V
V_{OL} output logic level low, (I_o = 4.0mA)[a] , 1.7V ≤ VDD ≤ 1.9V		-	-	0.4	V
V_{OH} output logic level high, (I_o = -4.0mA)[b] , 2.7V ≤ VDD ≤ 3.0V		VDD-0.2	-	-	V
V_{OH} output logic level high, (I_o = -4.0mA)[b] , 1.7V ≤ VDD ≤ 1.9V		VDD-0.4	-	-	V
Input and Tri-state Current with:					
Strong pull-up		-100	-40	-10	µA
Strong pull-down		10	40	100	µA
Weak pull-up		-5.0	-1.0	-0.2	µA
Weak pull-down		0.2	1.0	5.0	µA
I/O pad leakage current		-1	0	+1	µA
C_I input capacitance		1.0	-	5.0	pF

(a) Current sunk into terminal
(b) Current sourced out of terminal

3.5 USB Terminals

USB Terminals	Min	Typ	Max	Unit
VDD_USB for correct USB operation	3.1		3.6	V
Input Threshold				
V_{IL} input logic level low	-	-	0.3VDD_USB	V
V_{IH} input logic level high	0.7VDD_USB	-	-	V
Input Leakage Current				
VSS_PADS < VIN < VDD_USB[a]	-1	1	5	µA
C_I Input capacitance	2.5	-	10.0	pF
Output Voltage Levels to Correctly Terminated USB Cable				
V_{OL} output logic level low	0.0	-	0.2	V
V_{OH} output logic level high	2.8	-	VDD_USB	V

(a) Internal USB pull-up disabled

3.6 Power on Reset

Power-on Reset	Min	Typ	Max	Unit
VDD_CORE falling threshold	1.40	1.50	1.60	V
VDD_CORE rising threshold	1.50	1.60	1.70	V
Hysteresis	0.05	0.10	0.15	V

3.7 Auxilliary ADC

Auxiliary ADC		Min	Typ	Max	Unit
Resolution		-	-	8	Bits
Input voltage range (LSB size = VDD_ANA/255)		0	-	VDD_ANA	V
Accuracy	INL	-1	-	1	LSB
(Guaranteed monotonic)	DNL	0	-	1	LSB
Offset		-1	-	1	LSB
Gain Error		-0.8	-	0.8	%
Input Bandwidth		-	100	-	kHz
Conversion time		-	2.5	-	µs
Sample rate[a]		-	-	700	Samples/s

(a) ADC is accessed through the VM function. The sample rate given is achieved as part of this function

3.8 Auxilliary DAC

Auxiliary DAC	Min	Typ	Max	Unit
Resolution	-	-	8	Bits
Average output step size[a]	12.5	14.5	17.0	mV
Output Voltage		monotonic[a]		
Voltage range (I_O=0mA)	VSS_PADS	-	VDD_PIO	V
Current range	-10.0	-	0.1	mA
Minimum output voltage (I_O=100µA)	0.0	-	0.2	V
Maximum output voltage (I_O=10mA)	VDD_PIO-0.3	-	VDD_PIO	V
High Impedance leakage current	-1	-	1	µA
Offset	-220	-	120	mV
Integral non-linearity[a]	-2	-	2	LSB
Settling time (50pF load)	-	-	10	µs

[a] Specified for an output voltage between 0.2V and VDD_PIO -0.2V. Output is high impedance when chip is in Deep Sleep mode

3.9 Clocks

Crystal Oscillator	Min	Typ	Max	Unit
Crystal frequency[a]	8.0	-	32.0	MHz
Digital trim range[b]	5.0	6.2	8.0	pF
Trim step size[b]	-	0.1	-	pF
Transconductance	2.0	-	-	mS
Negative resistance[c]	870	1500	2400	Ω
External Clock				
Input frequency[d]	7.5	-	40.0	MHz
Clock input level[e]	0.2	-	VDD_ANA	V pk-pk
Allowable Jitter	-	-	15	ps rms
XTAL_IN input impedance	-	-	-	kΩ
XTAL_IN input capacitance	-	7	-	pF

(a) Integer multiple of 250kHz
(b) The difference between the internal capacitance at minimum and maximum settings of the internal digital trim
(c) XTAL frequency = 16MHz; XTAL C0 = 0.75pF; XTAL load capacitance = 8.5pF
(d) Clock input can be any frequency between 8MHz and 40MHz in steps of 250kHz plus CDMA/3G TCXO frequencies of 7.68, 14.44, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz
(e) Clock input can be either sinusoidal or square wave. If the peaks of the signal are below VSS_ANA or above VDD_ANA a DC blocking capacitor is required between the signal and XTAL_IN

Notes:

VDD_CORE, VDD_RADIO, VDD_LO and VDD_ANA are at 1.8V unless shown otherwise.

VDD_PADS, VDD_PIO and VDD_USB are at 3.0V unless shown otherwise.

The same setting of the digital trim is applied to both XTAL_IN and XTAL_OUT.

Current drawn into a pin is defined as positive; current supplied out of a pin is defined as negative.

3.10 Power Consumption

Operation Mode	Connection Type	UART Rate (kbps)	Average	Unit
Page scan, time interval 1.28s	-	115.2	0.43	mA
Inquiry and page scan	-	115.2	0.75	mA
ACL No traffic	Master	115.2	3.71	mA
ACL With file transfer	Master	115.2	8.44	mA
ACL No traffic	Slave	115.2	15.1	mA
ACL With file transfer	Slave	115.2	17.7	mA
ACL 40ms sniff	Master	38.4	1.58	mA
ACL 1.28s sniff	Master	38.4	0.14	mA
eSCO EV3 - Setting S1	Master	38.4	24.0	mA
SCO HV1	Master	38.4	36.3	mA
SCO HV3	Master	38.4	17.8	mA
SCO HV3 30ms sniff	Master	38.4	17.5	mA

Operation Mode	Connection Type	UART Rate (kbps)	Average	Unit
ACL 40ms sniff	Slave	38.4	1.39	mA
ACL 1.28s sniff	Slave	38.4	0.26	mA
eSCO EV3 - Setting S1	Slave	38.4	22.7	mA
SCO HV1	Slave	38.4	35.7	mA
SCO HV3	Slave	38.4	22.7	mA
SCO HV3 30ms sniff	Slave	38.4	16.8	mA
Parked 1.28s beacon	Slave	38.4	0.19	mA
Standby Host connection[(a)]	-	38.4	36	µA
Reset (RESETB low)[(a)]	-	-	49	µA

(a) Low power mode on the linear regulator is entered and exited automatically when the chip enters/leaves Deep Sleep mode. For more information about the electrical characteristics of the linear regulator, see section 3.3 in this document

Note:

Conditions: 20°C, 1.8V supply

4 Radio Characteristics - Basic Data Rate

4.1 Temperature +20°C

4.1.1 Transmitter

Radio Characteristics	VDD = 1.8V		Temperature = +20°C		
	Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power[a] [b]	-	4.5	-	-6 to +4[c]	dBm
RF power variation over temperature range with compensation enabled(±)[d]	-	1.5	-	-	dB
RF power variation over temperature range with compensation disabled(±)[d]	-	2.5	-	-	dB
RF power control range	-	35	-	≥16	dB
RF power range control resolution[e]	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	780	-	≤1000	kHz
Adjacent channel transmit power $F = F_0 \pm 2MHz$[f] [g]	-	-35	-	≤-20	dBm
Adjacent channel transmit power $F = F_0 \pm 3MHz$[f] [g]	-	-45	-	≤-40	dBm
Adjacent channel transmit power $F = F_0 \pm > 3MHz$[f] [g]	-	≤-50	-	≤-40	dBm
$\Delta f1_{avg}$ Maximum Modulation	-	165	-	$140<f1_{avg}<175$	kHz
$\Delta f2_{max}$ Minimum Modulation	-	152	-	115	kHz
$\Delta f1_{avg}/\Delta f2_{avg}$	-	0.98	-	≥0.80	-
Initial carrier frequency tolerance	-	8	-	±75	kHz
Drift Rate	-	7	-	≤20	kHz/50µs
Drift (single slot packet)	-	8	-	≤25	kHz
Drift (five slot packet)	-	9	-	≤40	kHz
2nd Harmonic Content	-	-45	-	≤-30	dBm
3rd Harmonic Content	-	-50	-	≤-30	dBm

(a) The BlueCore4-ROM firmware maintains the transmit power within Bluetooth v2.1 + EDR specification limits

(b) Measurement using PSKEY_LC_MAX_TX_POWER setting corresponding to a PSKEY_LC_POWER_TABLE power table entry = 63

(c) Class 2 RF transmit power range, Bluetooth specification v2.1 + EDR

(d) These parameters are dependent on matching circuit used, and its behaviour over temperature, therefore these parameters are not under CSR's direct control

(e) Resolution guaranteed over the range -5dB to -25dB relative to maximum power for Tx Level > 20

(f) Measured at F_0 = 2441MHz

(g) BlueCore4-ROM guaranteed to meet ACP performance in Bluetooth v2.1 + EDR specification, three exceptions allowed

Radio Characteristics	VDD = 1.8V	Temperature = +20°C				
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Cellular Band**	**Unit**
Emitted power in cellular bands measured at unbalanced port of the balun. Output power = 5dBm	0.869 - 0.894[a]	-	-125	-	GSM 850	dBm / Hz
	0.869 - 0.894[b]	-	-129	-	CDMA 850	
	0.925 - 0.960[a]	-	-129	-	GSM 900	
	1.570 - 1.580[c]	-	-135	-	GPS	
	1.805 - 1.880[a]	-	-133	-	GSM 1800 / DCS 1800	
	1.930 - 1.990[d]	-	-135	-	PCS 1900	
	1.930 - 1.990[a]	-	-133	-	GSM 1900	
	1.930 - 1.990[b]	-	-135	-	CDMA 1900	
	2.110 - 2.170[b]	-	-131	-	W-CDMA 2000	
	2.110 - 2.170[e]	-	-131	-	W-CDMA 2000	

(a) Integrated in 200kHz bandwidth and then normalised to 1Hz bandwidth
(b) Integrated in 1.2MHz bandwidth and then normalised to 1Hz bandwidth
(c) Integrated in 1MHz bandwidth and then normalised to 1Hz bandwidth
(d) Integrated in 30kHz bandwidth and then normalised to 1Hz bandwidth
(e) Integrated in 5MHz bandwidth and then normalised to 1Hz bandwidth

4.1.2 Receiver

Radio Characteristics		VDD = 1.8V		Temperature = +20°C		
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER for all packet types	2.402	-	-85.0	-	≤-70	dBm
	2.441	-	-84.0	-		
	2.480	-	-84.5	-		
Maximum received signal at 0.1% BER		-	>10	-	≥-20	dBm
	Frequency (MHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Continuous power required to block Bluetooth reception (for input power of -67dBm with 0.1% BER) measured at the unbalanced port of the balun.	30-2000	-	0	-	-10	dBm
	2000-2400	-	-10	-	-27	
	2500-3000	-	0	-	-27	
C/I co-channel		-	8	-	≤11	dB
Adjacent channel selectivity C/I $F = F_0 + 1MHz$ (a) (b)		-	-6	-	≤0	dB
Adjacent channel selectivity C/I $F = F_0 - 1MHz$ (a) (b)		-	-4	-	≤0	dB
Adjacent channel selectivity C/I $F = F_0 + 2MHz$ (a) (b)		-	-38	-	≤-30	dB
Adjacent channel selectivity C/I $F = F_0 - 2MHz$ (a) (b)		-	-24	-	≤-20	dB
Adjacent channel selectivity C/I $F = F_0 + 3MHz$ (a) (b)		-	-45	-	≤-40	dB
Adjacent channel selectivity C/I $F = F_0 - 5MHz$ (a) (b)		-	-45	-	≤-40	dB
Adjacent channel selectivity C/I $F = F_{Image}$ (a) (b)		-	-21	-	≤-9	dB
Maximum level of intermodulation interferers (c)		-	-30	-	≥-39	dBm
Spurious output level (d)		-	-160	-	-	dBm/Hz

(a) Up to five exceptions are allowed in v2.1 + EDR of the Bluetooth specification. BlueCore4-ROM is guaranteed to meet the C/I performance as specified by the Bluetooth specification v2.1 + EDR

(b) Measured at F = 2441MHz

(c) Measured at f1 - f2 = 5MHz. Measurement is performed in accordance with Bluetooth RF test RCV/CA/05/c., i.e., wanted signal at -64dBm

(d) Measured at unbalanced port of the balun. Integrated in 100kHz bandwidth and normalised to 1Hz. Actual figure is typically below -150dBm/Hz except for peaks of -70dbm at 1600MHz, -60dBm inband at 2.4GHz and -70dBm at 3.2GHz

Radio Characteristics	VDD = 1.8V	Temperature = +20°C				
	Frequency (GHz)	Min	Typ	Max	Cellular Band	Unit
Continuous power in cellular bands required to block Bluetooth reception (for input power of -67dBm with 0.1% BER) measured at the unbalanced port of the balun.	0.824 - 0.849	-	0[(a)]	-	GSM 850	dBm
	0.824 - 0.849	-	-10	-	CDMA 850	
	0.880 - 0.915	-	0	-	GSM 900	
	1.710 - 1.785	-	>0	-	GSM 1800 / DCS 1800	
	1.850 - 1.910	-	>0	-	GSM 1900 / PCS 1900	
	1.850 - 1.910	-	-12	-	CDMA 1900	
	1.920 - 1.980	-	-12	-	W-CDMA 2000	
Continuous power in cellular bands required to block Bluetooth reception (for input power of -72dBm with 0.1% BER) measured at the unbalanced port of the balun.	0.824 - 0.849	-	-2	-	GSM 850	dBm
	0.824 - 0.849	-	-13	-	CDMA 850	
	0.880 - 0.915	-	-5	-	GSM 900	
	1.710 - 1.785	-	0	-	GSM 1800 / DCS 1800	
	1.850 - 1.910	-	0	-	GSM 1900 / PCS 1900	
	1.850 - 1.910	-	-16	-	CDMA 1900	
	1.920 - 1.980	-	-18	-	W-CDMA 2000	

(a) 0 dBm if $f_{BLOCKING}$ < 0.831GHz

4.2 Temperature -40°C

4.2.1 Transmitter

Radio Characteristics	VDD = 1.8V		Temperature = -40°C		
	Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power[a]	-	5.5	-	-6 to +4[b]	dBm
RF power control range	-	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	780	-	≤1000	kHz
Adjacent channel transmit power $F = F_0 \pm 2MHz$[c] [d]	-	-35	-	≤-20	dBm
Adjacent channel transmit power $F = F_0 \pm 3MHz$[c] [d]	-	-43	-	≤-40	dBm
$\Delta f1_{avg}$ Maximum Modulation	-	165	-	$140<\Delta f1_{avg}<175$	kHz
$\Delta f2_{max}$ Minimum Modulation	-	154	-	115	kHz
$\Delta f2_{avg}/\Delta f1_{avg}$	-	0.99	-	≥0.80	-
Initial carrier frequency tolerance	-	9	-	±75	kHz
Drift Rate	-	6	-	≤20	kHz/50µs
Drift (single slot packet)	-	7	-	≤25	kHz
Drift (five slot packet)	-	9	-	≤40	kHz

(a) BlueCore4-ROM firmware maintains the transmit power to be within the Bluetooth v2.1 + EDR specification limits
(b) Class 2 RF transmit power range, Bluetooth v2.1 + EDR specification
(c) Measured at F_0 = 2441MHz
(d) Three exceptions are allowed in Bluetooth v2.1 + EDR specification

4.2.2 Receiver

Radio Characteristics		VDD = 1.8V		Temperature = -40°C		
	Frequency (GHz)	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.1% BER for all packet types	2.402	-	-87.0	-	≤-70	dBm
	2.441	-	-86.5	-		
	2.480	-	-87.0	-		
Maximum received signal at 0.1% BER		-	>10	-	≥-20	dBm

4.3 Temperature -25°C

4.3.1 Transmitter

Radio Characteristics	VDD = 1.8V		Temperature = -25°C		
	Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power[a]	-	5.0	-	-6 to +4[b]	dBm
RF power control range	-	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	780	-	≤1000	kHz
Adjacent channel transmit power $F = F_0 \pm 2MHz$[c] [d]	-	-32	-	≤-20	dBm
Adjacent channel transmit power $F = F_0 \pm 3MHz$[c] [d]	-	-43	-	≤-40	dBm
$\Delta f1_{avg}$ Maximum Modulation	-	165	-	$140<\Delta f1_{avg}<175$	kHz
$\Delta f2_{max}$ Minimum Modulation	-	152	-	≥115	kHz
$\Delta f2_{avg}/\Delta f1_{avg}$	-	0.98	-	≥0.80	-
Initial carrier frequency tolerance	-	9	-	±75	kHz
Drift Rate	-	7	-	≤20	kHz/50µs
Drift (single slot packet)	-	7	-	≤25	kHz
Drift (five slot packet)	-	9	-	≤40	kHz

(a) BlueCore4-ROM firmware maintains the transmit power to be within the Bluetooth v2.1 + EDR specification limits
(b) Class 2 RF transmit power range, Bluetooth v2.1 + EDR specification
(c) Measured at F_0 = 2441MHz
(d) Three exceptions are allowed in Bluetooth v2.1 + EDR specification

4.3.2 Receiver

Radio Characteristics		VDD = 1.8V		Temperature = -25°C		
	Frequency (GHz)	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.1% BER for all packet types	2.402	-	-86.5	-	≤-70	dBm
	2.441	-	-86.0	-		
	2.480	-	-86.5	-		
Maximum received signal at 0.1% BER		-	10	-	≥-20	dBm

4.4 Temperature +85°C

4.4.1 Transmitter

Radio Characteristics	VDD = 1.8V		Temperature = +85°C		
	Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power[a]	-	2.0	-	-6 to +4[b]	dBm
RF power control range	-	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	800	-	≤1000	kHz
Adjacent channel transmit power $F = F_0 \pm 2MHz$[c] [d]	-	-38	-	≤-20	dBm
Adjacent channel transmit power $F = F_0 \pm 3MHz$[c] [d]	-	-45	-	≤-40	dBm
$\Delta f1_{avg}$ Maximum Modulation	-	165	-	$140<\Delta f1_{avg}<175$	kHz
$\Delta f2_{max}$ Minimum Modulation	-	150	-	≥115	kHz
$\Delta f2_{avg}/\Delta f1_{avg}$	-	0.96	-	≥0.80	-
Initial carrier frequency tolerance	-	8	-	±75	kHz
Drift Rate	-	8	-	≤20	kHz/50µs
Drift (single slot packet)	-	8	-	≤25	kHz
Drift (five slot packet)	-	9	-	≤40	kHz

(a) BlueCore4-ROM firmware maintains the transmit power to be within the Bluetooth v2.1 + EDR specification limits
(b) Class 2 RF transmit power range, Bluetooth v2.1 + EDR specification
(c) Measured at F_0 = 2441MHz
(d) Three exceptions are allowed in Bluetooth v2.1 + EDR specification

4.4.2 Receiver

Radio Characteristics		VDD = 1.8V		Temperature = +85°C		
	Frequency (GHz)	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.1% BER for all packet types	2.402	-	-81.5	-	≤-70	dBm
	2.441	-	-81.0	-		
	2.480	-	-81.5	-		
Maximum received signal at 0.1% BER		-	>10	-	≥-20	dBm

4.5 Temperature +105°C

4.5.1 Transmitter

Radio Characteristics	VDD = 1.8V		Temperature = +105°C		
	Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power[a]	-	0	-	-6 to +4[b]	dBm
RF power control range	-	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	840	-	≤1000	kHz
Adjacent channel transmit power $F = F_0 \pm 2MHz$[c] [d]	-	-40	-	≤-20	dBm
Adjacent channel transmit power $F = F_0 \pm 3MHz$	-	-43	-	≤-40	dBm
$\Delta f1_{avg}$ Maximum Modulation	-	165	-	$140<\Delta f1_{avg}<175$	kHz
$\Delta f2_{max}$ Minimum Modulation	-	145	-	≥115	kHz
$\Delta f2_{avg}/\Delta f1_{avg}$	-	0.95	-	≥0.80	-
Initial carrier frequency tolerance	-	8	-	±75	kHz
Drift Rate	-	7	-	≤20	kHz/50µs
Drift (single slot packet)	-	8	-	≤25	kHz
Drift (five slot packet)	-	9	-	≤40	kHz

(a) BlueCore4-ROM firmware maintains the transmit power to be within the Bluetooth v2.1 + EDR specification limits
(b) Class 2 RF transmit power range, Bluetooth v2.1 + EDR specification
(c) Measured at F_0 = 2441MHz
(d) Three exceptions are allowed in the Bluetooth v2.1 + EDR specification

4.5.2 Receiver

Radio Characteristics		VDD = 1.8V		Temperature = +105°C		
	Frequency (GHz)	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.1% BER for all packet types	2.402	-	-80.5	-	≤-70	dBm
	2.441	-	-80.0	-		
	2.480	-	-80.5	-		
Maximum received signal at 0.1% BER		-	10	-	≥-20	dBm

5 Radio Characteristics - Enhanced Data Rate

Important Note:

Results shown are referenced to the unbalanced port of the balun.

5.1 Temperature +20°C

5.1.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +20°C						
		Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power[a]		-	1.5	-	-6 to +4[b]	dBm
Relative transmit power[c]		-	-1.2	-	-4 to +1	dB
π/4 DQPSK max carrier frequency stability[c] w_0		-	2	-	≤±10 for all blocks	kHz
π/4 DQPSK max carrier frequency stability[c] w_i		-	6	-	≤±75 for all blocks	kHz
π/4 DQPSK max carrier frequency stability[c] $\| w_0 + w_i \|$		-	8	-	≤±75 for all blocks	kHz
8DPSK max carrier frequency stability[c] w_0		-	2	-	≤±10 for all blocks	kHz
8DPSK max carrier frequency stability[c] w_i		-	6	-	≤±75 for all blocks	kHz
8DPSK max carrier frequency stability[c] $\| w_0 + w_i \|$		-	8	-	≤±75 for all blocks	kHz
π/4 DQPSK Modulation Accuracy[c] [d]	RMS DEVM	-	7	-	≤20	%
	99% DEVM	-	13	-	≤30	%
	Peak DEVM	-	19	-	≤35	%
8DPSK Modulation Accuracy[c] [d]	RMS DEVM	-	7	-	≤13	%
	99% DEVM	-	13	-	≤20	%
	Peak DEVM	-	17	-	≤25	%
In-band spurious emissions[e]	$F>F_0$ +3MHz	-	<-50	-	≤-40	dBm
	$F<F_0$ -3MHz	-	<-50	-	≤-40	dBm
	$F=F_0$ -3MHz	-	-46	-	≤-40	dBm
	$F=F_0$ -2MHz	-	-34	-	≤-20	dBm
	$F=F_0$ -1MHz	-	-35	-	≤-26	dB
	$F=F_0$ +1MHz	-	-35	-	≤-26	dB
	$F=F_0$ +2MHz	-	-31	-	≤-20	dBm
	$F=F_0$ +3MHz[e]	-	-33	-	≤-40	dBm
EDR Differential Phase Encoding		99	No Errors	-	≥99	%

(a) BlueCore4-ROM firmware maintains transmit power within Bluetooth v2.1 + EDR specification limits
(b) Class 2 RF transmit power range, Bluetooth v2.1 + EDR specification
(c) Measurements methods are in accordance with the Bluetooth v2.1 + EDR specification
(d) Modulation accuracy utilises *differential error vector magnitude* (DEVM) with tracking of the frequency drift
(e) Bluetooth specification values are for 8DPSK. Three exceptions are allowed in Bluetooth v2.1 + EDR specification

5.1.2 Receiver

Radio Characteristics	VDD = 1.8V	Temperature = +20°C				
	Modulation	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.01% BER[a]	π/4 DQPSK	-	-87		≤-70	dBm
	8DPSK	-	-78		≤-70	dBm
Maximum received signal at 0.1% BER[a]	π/4 DQPSK	-	-8	-	≥-20	dBm
	8DPSK	-	-10	-	≥-20	dBm
C/I co-channel at 0.1% BER[a]	π/4 DQPSK	-	10	-	≤+13	dB
	8DPSK	-	19	-	≤+21	dB
Adjacent channel selectivity	π/4 DQPSK	-	-10	-	≤0	dB
C/I $F=F_0+1MHz$[a] [b] [c]	8DPSK	-	-5	-	≤+5	dB
Adjacent channel selectivity	π/4 DQPSK	-	-11	-	≤0	dB
C/I $F=F_0-1MHz$ [a] [b] [c]	8DPSK	-	-5	-	≤+5	dB
Adjacent channel selectivity	π/4 DQPSK	-	-40	-	≤-30	dB
C/I $F=F_0+2MHz$[a] [b] [c]	8DPSK	-	-40	-	≤-25	dB
Adjacent channel selectivity	π/4 DQPSK	-	-23	-	≤-20	dB
C/I $F=F_0-2MHz$[a] [b] [c]	8DPSK	-	-20	-	≤-13	dB
Adjacent channel selectivity	π/4 DQPSK	-	-45	-	≤-40	dB
C/I $F\geq F_0+3MHz$[a] [b] [c]	8DPSK	-	-45	-	≤-33	dB
Adjacent channel selectivity	π/4 DQPSK	-	-45	-	≤-40	dB
C/I $F\leq F_0-5MHz$[a] [b] [c]	8DPSK	-	-45	-	≤-33	dB
Adjacent channel selectivity	π/4 DQPSK	-	-20	-	≤-7	dB
C/I $F=F_{Image}$[a] [b] [c]	8DPSK	-	-15	-	≤0	dB

(a) Measurements methods are in accordance with the Bluetooth v2.1 + EDR specification

(b) Up to five exceptions are allowed in the Bluetooth v2.1 + EDR specification.BlueCore4-ROM is guaranteed to meet the C/I performance as specified by the Bluetooth v2.1 + EDR

(c) Measured at F_0 = 2405MHz, 2441MHz, 2477MHz

5.2 Temperature -40°C

5.2.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = -40°C						
		Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power[a]		-	4	-	-6 to +4[b]	dBm
Relative transmit power[c]		-	-1.2	-	-4 to +1	dB
π/4 DQPSK max carrier frequency stability[c] w_0		-	2	-	≤±10 for all blocks	kHz
π/4 DQPSK max carrier frequency stability[c] w_i		-	7	-	≤±75 for all blocks	kHz
π/4 DQPSK max carrier frequency stability[c] $\| w_0+w_i \|$		-	8	-	≤±75 for all blocks	kHz
8DPSK max carrier frequency stability[c] w_0		-	3	-	≤±10 for all blocks	kHz
8DPSK max carrier frequency stability[c] w_i		-	7	-	≤±75 for all blocks	kHz
8DPSK max carrier frequency stability[c] $\| w_0+ w_i \|$		-	9	-	≤±75 for all blocks	kHz
π/4 DQPSK Modulation Accuracy[c] [d]	RMS DEVM	-	7	-	≤20	%
	99% DEVM	-	14	-	≤30	%
	Peak DEVM	-	19	-	≤35	%
8DPSK Modulation Accuracy[c] [d]	RMS DEVM	-	6	-	≤13	%
	99% DEVM	-	12	-	≤20	%
	Peak DEVM	-	18	-	≤25	%
In-band spurious emissions[e]	$F>F_0$+3MHz	-	<-50	-	≤-40	dBm
	$F<F_0$-3MHz	-	<-50	-	≤-40	dBm
	$F=F_0$-3MHz	-	-42	-	≤-40	dBm
	$F=F_0$-2MHz	-	-25	-	≤-20	dBm
	$F=F_0$-1MHz	-	-32	-	≤-26	dB
	$F=F_0$+1MHz	-	-33	-	≤-26	dB
	$F=F_0$+2MHz	-	-25	-	≤-20	dBm
	$F=F_0$+3MHz[e]	-	-30	-	≤-40	dBm
EDR Differential Phase Encoding		99	No Errors	-	≥99	%

(a) BlueCore4-ROM firmware maintains transmit power within Bluetooth v2.1 + EDR specification limits
(b) Class 2 RF transmit power range, Bluetooth v2.1 + EDR specification
(c) Measurements methods are in accordance with the Bluetooth v2.1 + EDR specification
(d) Modulation accuracy utilises *differential error vector magnitude* (DEVM) with tracking of the frequency drift
(e) The Bluetooth specification values are for 8DPSK. Up to three exceptions are allowed in the Bluetooth v2.1 + EDR specification

5.2.2 Receiver

Radio Characteristics	VDD = 1.8V	Temperature = -40°C				
	Modulation	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.01% BER[a]	π/4 DQPSK	-	-85	-	≤-70	dBm
	8DPSK	-	-78	-	≤-70	dBm
Maximum received signal at 0.1% BER[a]	π/4 DQPSK	-	-12	-	≤-20	dBm
	8DPSK	-	-15	-	≤-20	dBm

[a] Measurements methods are in accordance with the Bluetooth v2.1 + EDR specification

5.3 Temperature -25°C

5.3.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = -25°C						
		Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power[a]		-	3	-	-6 to +4[b]	dBm
Relative transmit power[c]		-	-1.2	-	-4 to +1	dB
π/4 DQPSK max carrier frequency stability[c] w_0		-	2	-	≤±10 for all blocks	kHz
π/4 DQPSK max carrier frequency stability[c] w_i		-	6	-	≤±75 for all blocks	kHz
π/4 DQPSK max carrier frequency stability[c] $\| w_0+w_i \|$		-	8	-	≤±75 for all blocks	kHz
8DPSK max carrier frequency stability[c] w_0		-	2	-	≤±10 for all blocks	kHz
8DPSK max carrier frequency stability[c] w_i		-	6	-	≤±75 for all blocks	kHz
8DPSK max carrier frequency stability[c] $\| w_0+ w_i \|$		-	8	-	≤±75 for all blocks	kHz
π/4 DQPSK Modulation Accuracy[c] [d]	RMS DEVM	-	6	-	≤20	%
	99% DEVM	-	13	-	≤30	%
	Peak DEVM	-	16	-	≤35	%
8DPSK Modulation Accuracy[c] [d]	RMS DEVM	-	6	-	≤13	%
	99% DEVM	-	11	-	≤20	%
	Peak DEVM	-	16	-	≤25	%
In-band spurious emissions[e]	$F>F_0+3MHz$	-	<-50	-	≤-40	dBm
	$F<F_0-3MHz$	-	<-50	-	≤-40	dBm
	$F=F_0-3MHz$	-	-43	-	≤-40	dBm
	$F=F_0-2MHz$	-	-29	-	≤-20	dBm
	$F=F_0-1MHz$	-	-32	-	≤-26	dB
	$F=F_0+1MHz$	-	-33	-	≤-26	dB
	$F=F_0+2MHz$	-	-27	-	≤-20	dBm
	$F=F_0+3MHz$[e]	-	-31	-	≤-40	dBm
EDR Differential Phase Encoding		99	No Errors	-	≥99	%

(a) BlueCore4-ROM firmware maintains transmit power within Bluetooth v2.1 + EDR specification limits
(b) Class 2 RF transmit power range, Bluetooth v2.1 + EDR specification
(c) Measurements methods are in accordance with the Bluetooth v2.1 + EDR specification
(d) Modulation accuracy utilises *differential error vector magnitude* (DEVM) with tracking of the frequency drift
(e) The Bluetooth specification values are for 8DPSK. Up to three exceptions are allowed in the Bluetooth v2.1 + EDR specification

5.3.2 Receiver

Radio Characteristics	VDD = 1.8V	Temperature = -25°C				
	Modulation	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.01% BER(a)	π/4 DQPSK	-	-85	-	≤-70	dBm
	8DPSK	-	-78	-	≤-70	dBm
Maximum received signal at 0.1% BER(a)	π/4 DQPSK	-	-12	-	≤-20	dBm
	8DPSK	-	-15	-	≤20	dBm

(a) Measurements methods are in accordance with the Bluetooth v2.1 + EDR specification

5.4 Temperature +85°C

5.4.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +85°C						
		Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power[a]		-	-2	-	-6 to +4[b]	dBm
Relative transmit power[c]		-	-1.2	-	-4 to +1	dB
π/4 DQPSK max carrier frequency stability[c] w_0		-	2	-	≤±10 for all blocks	kHz
π/4 DQPSK max carrier frequency stability[c] w_i		-	7	-	≤±75 for all blocks	kHz
π/4 DQPSK max carrier frequency stability[c] $I w_0+w_i I$		-	9	-	≤±75 for all blocks	kHZ
8DPSK max carrier frequency stability[c] w_0		-	2	-	≤±10 for all blocks	kHZ
8DPSK max carrier frequency stability[c] w_i		-	7	-	≤±75 for all blocks	kHZ
8DPSK max carrier frequency stability[c] $I w_0+ w_i I$		-	9	-	≤±75 for all blocks	kHZ
π/4 DQPSK Modulation Accuracy[c] [d]	RMS DEVM	-	6	-	≤20	%
	99% DEVM	-	13	-	≤30	%
	Peak DEVM	-	16	-	≤35	%
8DPSK Modulation Accuracy[c] [d]	RMS DEVM	-	6	-	≤13	%
	99% DEVM	-	11	-	≤20	%
	Peak DEVM	-	16	-	≤25	%
In-band spurious emissions[e]	$F>F_0+3MHz$	-	<-50	-	≤-40	dBm
	$F<F_0-3MHz$	-	<-50	-	≤-40	dBm
	$F=F_0-3MHz$	-	-43	-	≤-40	dBm
	$F=F_0-2MHz$	-	-29	-	≤-20	dBm
	$F=F_0-1MHz$	-	-32	-	≤-26	dB
	$F=F_0+1MHz$	-	-33	-	≤-26	dB
	$F=F_0+2MHz$	-	-27	-	≤-20	dBm
	$F=F_0+3MHz$[e]	-	-31	-	≤-40	dBm
EDR Differential Phase Encoding		99	No Errors	-	≥99	%

(a) BlueCore4-ROM firmware maintains transmit power within Bluetooth v2.1 + EDR specification limits
(b) Class 2 RF transmit power range, Bluetooth v2.1 + EDR specification
(c) Measurements methods are in accordance with the Bluetooth v2.1 + EDR specification
(d) Modulation accuracy utilises *differential error vector magnitude* (DEVM) with tracking of the frequency drift
(e) The Bluetooth specification values are for 8DPSK. Up to three exceptions are allowed in the Bluetooth v2.1 + EDR specification

5.4.2 Receiver

Radio Characteristics	VDD = 1.8V	Temperature = +85°C				
	Modulation	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.01% BER[a]	π/4 DQPSK	-	-83	-	≤-70	dBm
	8DPSK	-	-75	-	≤-70	dBm
Maximum received signal at 0.1% BER[a]	π/4 DQPSK	-	-5	-	≤-20	dBm
	8DPSK	-	-5	-	≤-20	dBm

(a) Measurements methods are in accordance with the Bluetooth v2.1 + EDR specification

5.5 Temperature +105°C

5.5.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +105°C						
		Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power[a]		-	-3	-	-6 to +4[b]	dBm
Relative transmit power[c]		-	-1.3	-	-4 to +1	dB
π/4 DQPSK max carrier frequency stability[c] w_0		-	1	-	≤±10 for all blocks	kHz
π/4 DQPSK max carrier frequency stability[c] w_i		-	7	-	≤±75 for all blocks	kHz
π/4 DQPSK max carrier frequency stability[c] $\| w_0+w_i \|$		-	8	-	≤±75 for all blocks	kHz
8DPSK max carrier frequency stability[c] w_0		-	1	-	≤±10 for all blocks	kHz
8DPSK max carrier frequency stability[c] w_i		-	7	-	≤±75 for all blocks	kHz
8DPSK max carrier frequency stability[c] $\| w_0+ w_i \|$		-	8	-	≤±75 for all blocks	kHz
π/4 DQPSK Modulation Accuracy[c] [d]	RMS DEVM	-	7	-	≤20	%
	99% DEVM	-	12	-	≤30	%
	Peak DEVM	-	16	-	≤35	%
8DPSK Modulation Accuracy[c] [d]	RMS DEVM	-	7	-	≤13	%
	99% DEVM	-	12	-	≤20	%
	Peak DEVM	-	15	-	≤25	%
In-band spurious emissions[e]	$F>F_0+3MHz$	-	<-50	-	≤-40	dBm
	$F<F_0-3MHz$	-	<-50	-	≤-40	dBm
	$F=F_0-3MHz$	-	-51	-	≤-40	dBm
	$F=F_0-2MHz$	-	-45	-	≤-20	dBm
	$F=F_0-1MHz$	-	-37	-	≤-26	dB
	$F=F_0+1MHz$	-	-32	-	≤-26	dB
	$F=F_0+2MHz$	-	-37	-	≤-20	dBm
	$F=F_0+3MHz$[e]	-	-38	-	≤-40	dBm
EDR Differential Phase Encoding		99	No Errors	-	≥99	%

(a) BlueCore4-ROM firmware maintains transmit power within Bluetooth v2.1 + EDR specification limits
(b) Class 2 RF transmit power range, Bluetooth v2.1 + EDR specification
(c) Measurements methods are in accordance with the Bluetooth v2.1 + EDR specification
(d) Modulation accuracy utilises *differential error vector magnitude* (DEVM) with tracking of the frequency drift
(e) The Bluetooth specification values are for 8DPSK. Up to three exceptions are allowed in the Bluetooth v2.1 + EDR specification

5.5.2 Receiver

Radio Characteristics	VDD = 1.8V	Temperature = +105°C				
	Modulation	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.01% BER[a]	π/4 DQPSK	-	-85	-	≤-70	dBm
	8DPSK	-	-73	-	≤-70	dBm
Maximum received signal at 0.1% BER[a]	π/4 DQPSK	-	-5	-	≤-20	dBm
	8DPSK	-	-5	-	≤-20	dBm

(a) Measurements methods are in accordance with the Bluetooth v2.1 + EDR specification

6 Device Diagram

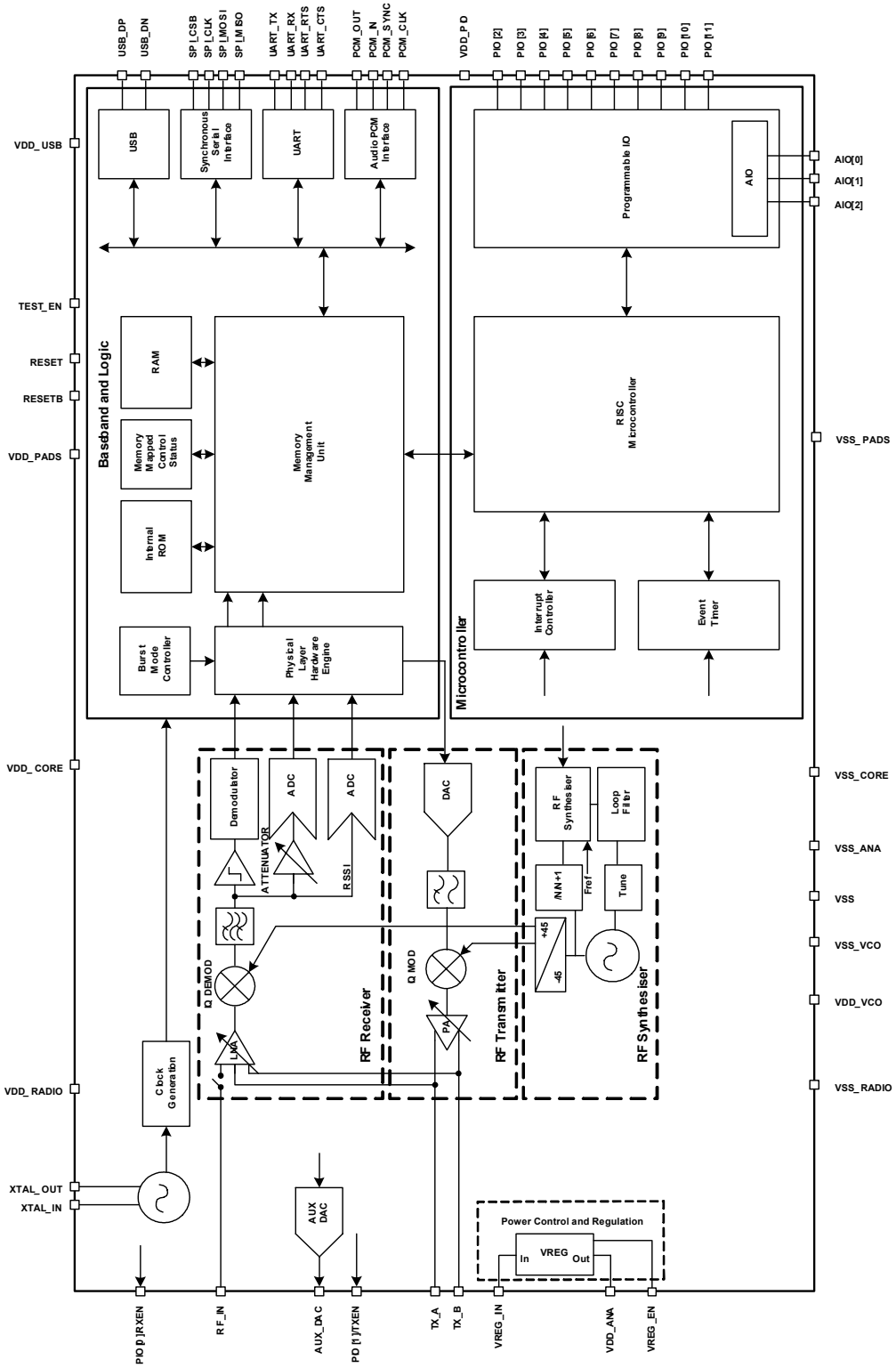


Figure 6.1: BlueCore4-ROM BGA Device Diagram

7 Description of Functional Blocks

7.1 RF Receiver

The receiver features a near-zero *Intermediate Frequency* (IF) architecture that allows the channel filters to be integrated onto the die. Sufficient out-of-band blocking specification at the *Low Noise Amplifier* (LNA) input allows the radio to be used in close proximity to *Global System for Mobile Communications* (GSM) and *Wideband Code Division Multiple Access* (W-CDMA) cellular phone transmitters without being desensitised. The use of a digital *Frequency Shift Keying* (FSK) discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows BlueCore4-ROM to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

For EDR, an ADC is used to digitise the IF received signal.

7.1.1 Low Noise Amplifier

The LNA can be configured to operate in single-ended or differential mode. Single-ended mode is used for Class 1 Bluetooth operation; differential mode is used for Class 2 operation.

7.1.2 Analogue to Digital Converter

The *Analogue to Digital Converter* (ADC) is used to implement fast *Automatic Gain Control* (AGC). The ADC samples the *Received Signal Strength Indicator* (RSSI) voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference limited environments.

7.2 RF Transmitter

7.2.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise the frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

7.2.2 Power Amplifier

The internal *Power Amplifier* (PA) has a maximum output power of +6dBm. This allows BlueCore4-ROM to be used in Class 2 and Class 3 radios without an external RF PA.

Support for transmit power control allows a simple implementation for Class 1 with an external RF PA.

7.2.3 Auxiliary DAC

An 8-bit voltage Auxiliary DAC is provided for power control of an external PA for Class 1 operation or any other customer specific application.

7.3 RF Synthesiser

The radio synthesiser is fully integrated onto the die with no requirement for an external *Voltage Controlled Oscillator* (VCO) screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth v2.0 + EDR specification.

7.4 Power Control and Regulation

BlueCore4-ROM contains a 1.8V linear regulator which can be used to power the complete chip.

7.5 Clock Input and Generation

The reference clock for the system is generated from a TCXO or crystal input between 8MHz and 40MHz. All internal reference clocks are generated using a phase locked loop, which is locked to the external reference frequency.

7.6 Baseband and Logic

7.6.1 Memory Management Unit

The *Memory Management Unit* (MMU) provides a number of dynamically allocated ring buffers that hold the data that is in transit between the host and the air. The dynamic allocation of memory ensures efficient use of the available *Random Access Memory* (RAM) and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers.

7.6.2 Burst Mode Controller

During radio transmission the *Burst Mode Controller* (BMC) constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During radio reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

7.6.3 Physical Layer Hardware Engine DSP

Dedicated logic is used to perform the following:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

The following voice data translations and operations are performed by firmware:

- A-law/μ-law/linear voice data (from host)
- A-law/μ-law/*Continuously Variable Slope Delta* (CVSD) (over the air)
- Voice interpolation for lost packets
- Rate mismatches

The hardware supports all mandatory and optional features of the Bluetooth v2.0 + EDR specification.

7.6.4 System RAM

48KB of on-chip RAM is provided to support the RISC MCU and is shared between the ring buffers used to hold voice/data for each active connection and the general purpose memory required by the Bluetooth stack.

7.6.5 ROM

4Mbits of metal programmable ROM is provided for system firmware implementation.

7.6.6 USB

This is a full speed *Universal Serial Bus* (USB) interface for communicating with other compatible digital devices. BlueCore4-ROM acts as a USB peripheral, responding to requests from a master host controller such as a PC.

7.6.7 Synchronous Serial Interface

This is a synchronous *serial port interface* (SPI) for interfacing with other digital devices. The SPI port can be used for system debugging.

7.6.8 UART

This is a standard *Universal Asynchronous Receiver Transmitter* (UART) interface for communicating with other serial devices.

7.6.9 Audio PCM Interface

The audio *pulse code modulation* (PCM) interface supports continuous transmission and reception of PCM encoded audio data over Bluetooth.

7.7 Microcontroller

The *microcontroller unit* (MCU), interrupt controller and event timer run the Bluetooth software stack and control the radio and host interfaces. A 16-bit *reduced instruction set computer* (RISC) microcontroller is used for low power consumption and efficient use of memory.

7.7.1 Programmable I/O

BlueCore4-ROM has a total of 15 (12 digital and 3 analogue) programmable I/O terminals. These are controlled by firmware running on the device.

7.7.2 802.11 Co-Existence Interface

Dedicated hardware is provided to implement a variety of 802.11 (Wi-Fi) co-existence schemes. Channel skipping AFH, priority signalling, channel signalling and host passing of channel instructions are all supported. The features are configured in firmware. The details of some methods are proprietary (e.g., Intel WCS). Contact CSR for details.

8 CSR Bluetooth Software Stacks

BlueCore4-ROM is supplied with Bluetooth v2.1 + EDR compliant stack firmware, which runs on the internal RISC microcontroller.

The BlueCore4-ROM software architecture allows Bluetooth processing and the application program to be shared in different ways between the internal RISC microcontroller and an external host processor (if any). The upper layers of the Bluetooth stack (above HCI) can be run either on-chip or on the host processor.

8.1 BlueCore HCI Stack

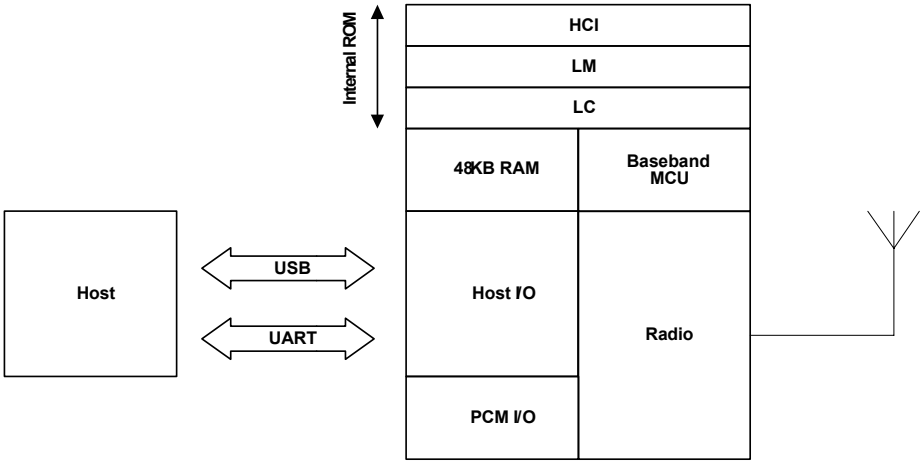


Figure 8.1: BlueCore HCI Stack

In the implementation shown in Figure 8.1 the internal processor runs the Bluetooth stack up to the *Host Controller Interface* (HCI). The Host processor must provide all upper layers including the application.

8.1.1 Key Features of the HCI Stack: Standard Bluetooth Functionality

CSR supports the following BlueCore v2.1 + EDR functionality:

- Secure simple pairing
- Sniff subrating
- Encryption pause resume
- Packet boundary flags
- Encryption
- Extended inquiry response

CSR supports the following Bluetooth v2.0 + EDR mandatory functionality:

- *Adaptive Frequency Hopping* (AFH), including classifier
- Faster connection - enhanced inquiry scan (immediate FHS response)
- LMP improvements
- Parameter ranges

Optional Bluetooth v2.0 + EDR functionality supported:

- *Adaptive Frequency Hopping* (AFH) as Master and Automatic Channel Classification
- Fast Connect - Interlaced Inquiry and Page Scan plus RSSI during Inquiry
- Extended SCO (eSCO), eV3 +CRC, eV4, eV5
- SCO handle
- Synchronisation

The firmware was written against the Bluetooth v2.0 + EDR specification.

- Bluetooth components:
  - Baseband (including LC)
  - LM
  - HCI
- Standard USB v1.1 and UART HCI Transport Layers
- All standard radio packet types
- Full Bluetooth data rate, enhanced data rates of 2 and 3Mbps(1)
- Operation with up to seven active slaves(1)
- Scatternet v2.5 operation
- Maximum number of simultaneous active ACL connections: 7(2)
- Maximum number of simultaneous active SCO connections: 3(2)
- Operation with up to three SCO links, routed to one or more slaves
- All standard SCO voice coding, plus transparent SCO
- Standard operating modes: Page, Inquiry, Page-Scan and Inquiry-Scan
- All standard pairing, authentication, link key and encryption operations
- Standard Bluetooth power saving mechanisms: Hold, Sniff and Park modes, including Forced Hold
- Dynamic control of peers' transmit power via LMP
- Master/Slave switch
- Broadcast
- Channel quality driven data rate
- All standard Bluetooth test modes

The firmware's supported Bluetooth features are detailed in the standard *Protocol Implementation Conformance Statement* (PICS) documents, available from www.csr.com.

(1) This is the maximum allowed by Bluetooth v2.0 + EDR specification.

(2) BlueCore4-ROM supports all combinations of active ACL and SCO channels for both master and slave operation, as specified by the Bluetooth v2.0 + EDR specification.

8.1.2 Key Features of the HCI Stack: Extra Functionality

The firmware extends the standard Bluetooth functionality with the following features:

- Supports *BlueCore Serial Protocol* (BCSP), a proprietary, reliable alternative to the standard Bluetooth UART Host Transport
- Provides a set of approximately 50 manufacturer-specific HCI extension commands. This command set, called *BlueCore Command* (BCCMD), provides:
  - Access to the chip's general-purpose PIO port
  - The negotiated effective encryption key length on established Bluetooth links
  - Access to the firmware's random number generator
  - Controls to set the default and maximum transmit powers; these can help minimise interference between overlapping, fixed-location piconets
  - Dynamic UART configuration
  - Radio transmitter enable/disable. A simple command connects to a dedicated hardware switch that determines whether the radio can transmit.
- The firmware can read the voltage on a pair of the chip's external pins. This is normally used to build a battery monitor, using either VM or host code
- A block of BCCMD commands provides access to the chip's Persistent Store configuration database (PS). The database sets the device's Bluetooth address, Class of Device, radio (transmit class) configuration, SCO routing, LM, USB and DFU constants, etc.
- A UART break condition can be used in three ways:
  1. Presenting a UART break condition to the chip can force the chip to perform a hardware reboot
  2. Presenting a break condition at boot time can hold the chip in a low power state, preventing normal initialisation while the condition exists
  3. With BCSP, the firmware can be configured to send a break to the host before sending data. (This is normally used to wake the host from a Deep Sleep state.)
- The DFU standard has been extended with public/private key authentication, allowing manufacturers to control the firmware that can be loaded onto their Bluetooth modules
- A modified version of the DFU protocol allows firmware upgrade via the chip's UART
- A block of radio test or BIST commands allows direct control of the chip's radio. This aids the development of modules' radio designs, and can be used to support Bluetooth qualification.
- *Virtual Machine* (VM). The firmware provides the VM environment in which to run application-specific code. Although the VM is mainly used with BlueLab and RFCOMM builds (alternative firmware builds providing L2CAP, SDP and RFCOMM), the VM can be used with this build to perform simple tasks such as flashing LEDs via the chip's PIO port.
- Hardware low power modes: Shallow Sleep and Deep Sleep. The chip drops into modes that significantly reduce power consumption when the software goes idle.
- SCO channels are normally routed via HCI (over BCSP). However, up to three SCO channels can be routed over the chip's single PCM port (at the same time as routing any remaining SCO channels over HCI).

Note:

Always refer to the Firmware Release Note for the specific functionality of a particular build.

8.2 BlueCore RFCOMM Stack

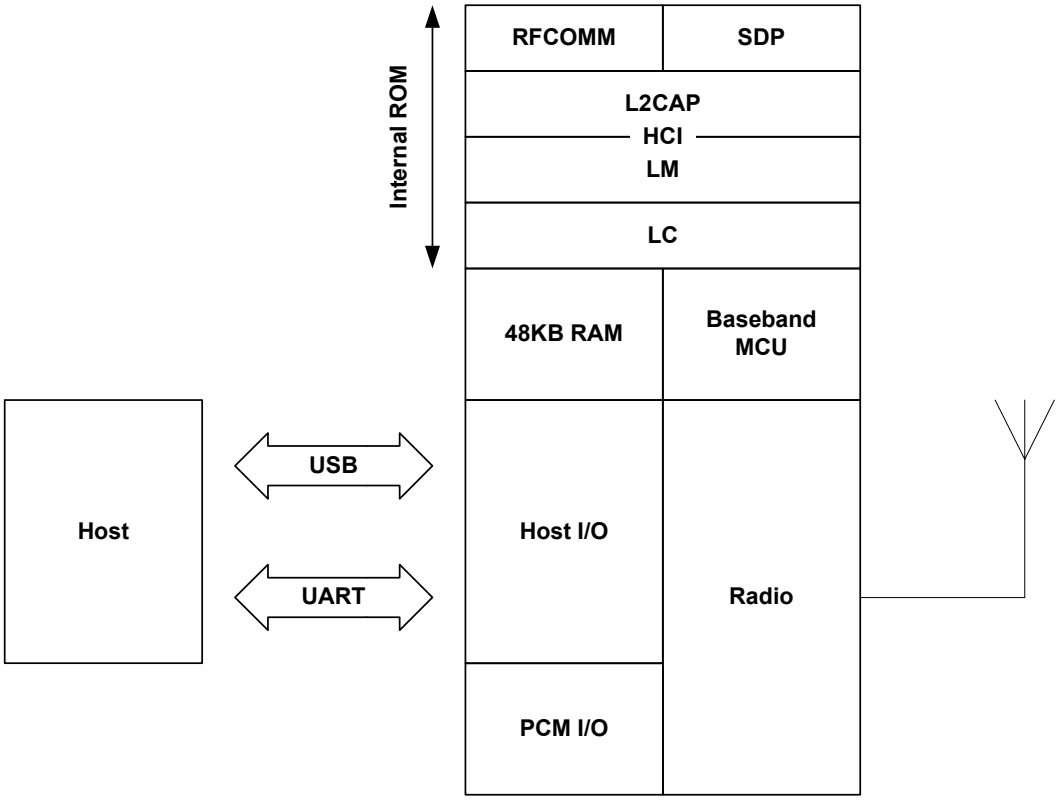


Figure 8.2: BlueCore RFCOMM Stack

In the version of the firmware, shown in Figure 8.2 the upper layers of the Bluetooth stack up to RFCOMM are run on-chip. This reduces host-side software and hardware requirements at the expense of some of the power and flexibility of the HCI only stack.

8.2.1 Key Features of the RFCOMM Stack

Interfaces to Host:

- RFCOMM, an RS-232 serial cable emulation protocol
- SDP, a service database look-up protocol

Connectivity:

- Maximum number of active slaves: three
- Maximum number of simultaneous active ACL connections: three
- Maximum number of simultaneous active SCO connections: three
- Data Rate: up to 350kbps(1)

Security:

- Full support for all Bluetooth security features up to and including strong (128-bit) encryption.

Power Saving:

- Full support for all Bluetooth power saving modes (Park, Sniff and Hold).

Data Integrity:

- CQDDR increases the effective data rate in noisy environments.
- RSSI used to minimise interference to other radio devices using the ISM band.

(1) The data rate is with respect to BlueCore4-ROM with basic data rate packets.

8.3 BlueCore Virtual Machine Stack

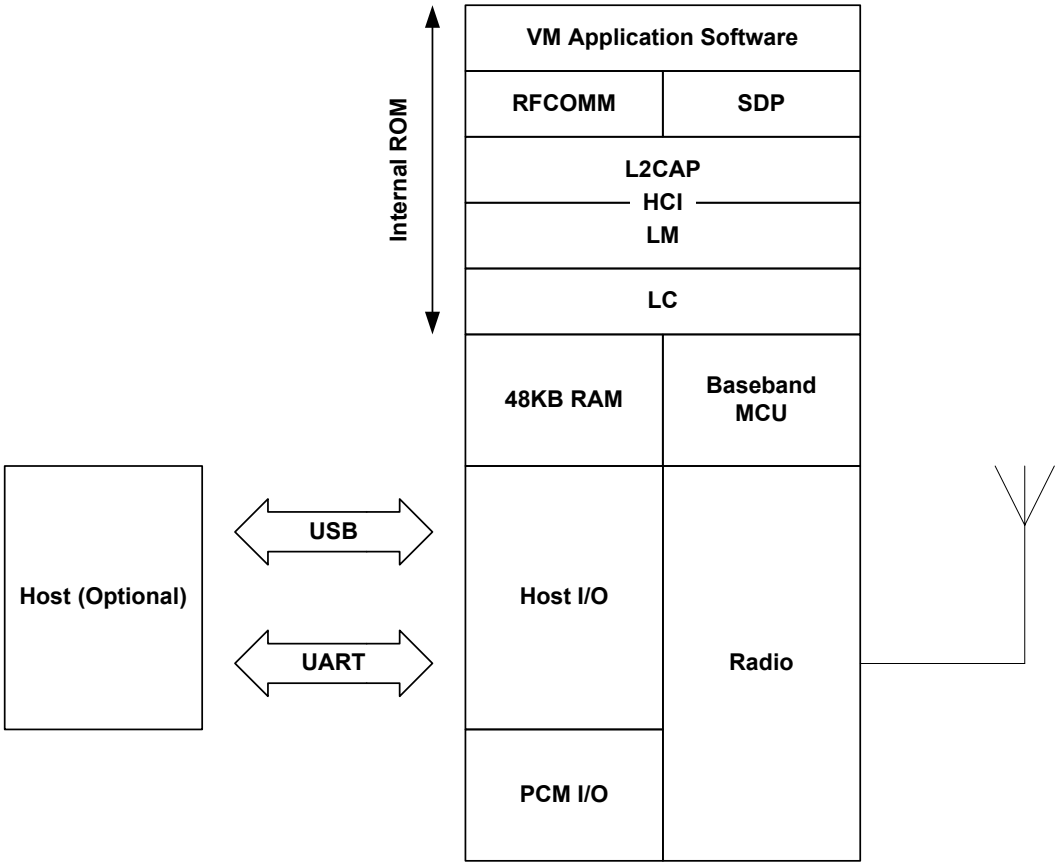


Figure 8.3: Virtual Machine

In Figure 8.3, this version of the stack firmware shown requires no host processor (but it can use a host processor for debugging, etc.). All software layers, including application software, run on the internal RISC processor in a protected user software execution environment known as a *Virtual Machine* (VM).

The user may write custom application code to run on the BlueCore VM using BlueLab SDK supplied with the BlueLab Multimedia and Casira development kits, available separately from CSR. This code will then execute alongside the main BlueCore firmware. The user is able to make calls to the BlueCore firmware for various operations.

The execution environment is structured so the user application does not adversely affect the main software routines, thus ensuring that the Bluetooth stack software component does not need re-qualification when the application is changed.

Using the VM and the BlueLab SDK the user is able to develop applications such as a cordless handsfree kit or other profiles without the requirement of a host controller. BlueLab is supplied with example code including a full implementation of the handsfree profile.

Note:

Sample applications to control PIO lines can also be written with BlueLab SDK and the VM for the HCI stack.

8.4 Additional Software for Other Embedded Applications

When the upper layers of the Bluetooth protocol stack are run as firmware on BlueCore4-ROM, a UART software driver is supplied that presents the L2CAP, RFCOMM and *Service Discovery Protocol* (SDP) APIs to higher Bluetooth stack layers running on the host. The code is provided as C source or object code.

8.5 CSR Development Systems

CSR's BlueLab Multimedia and Casira development kits are available to allow the evaluation of the BlueCore4-ROM hardware and software, and as toolkits for developing on-chip and host software.

9 Device Terminal Descriptions

9.1 RF Ports

The BlueCore4-ROM RF_IN terminal can be configured as either a single-ended or differential input. The operational mode is determined by setting PSKEY_TXRX_PIO_CONTROL (0x20).

9.1.1 TX_A and TX_B

TX_A and TX_B form a complementary balanced pair. On transmit, their outputs are combined using a balun into the single-ended output required for the antenna. Similarly, on receive, their input signals are combined internally. Both terminals present similar complex impedances that require matching networks between them and the balun. Starting from the substrate (chip) side, the outputs can each be modelled as an ideal current source in parallel with a lossy resistance and a capacitor. The bond wire can be represented as series inductance.

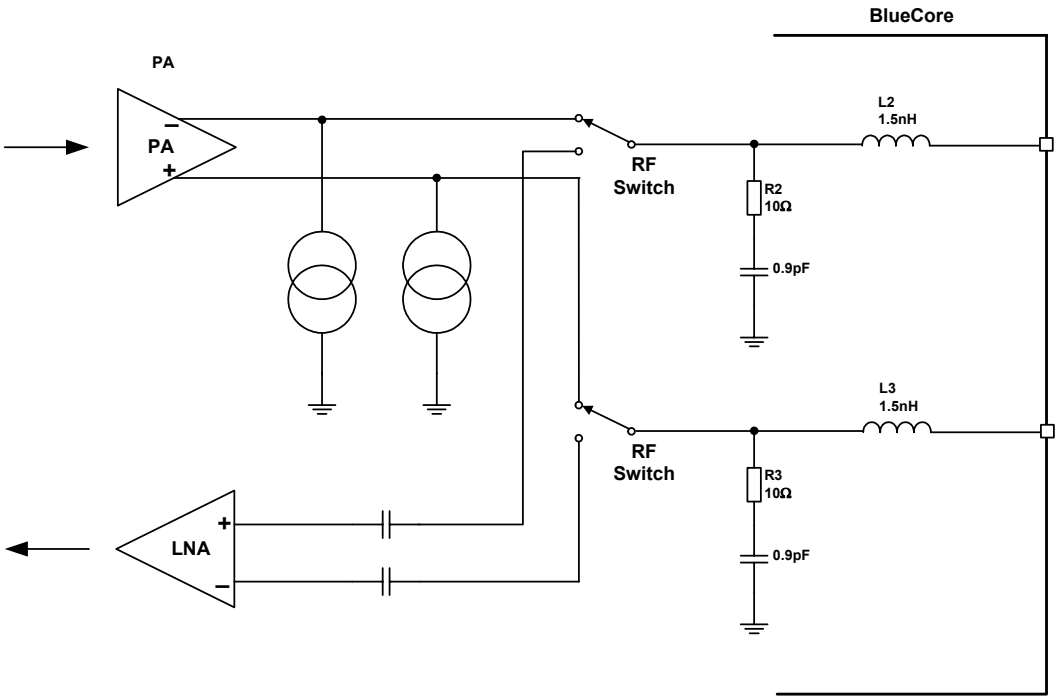


Figure 9.1: Circuit TX_A and TX_B

9.1.2 Single-Ended Input

This is the single-ended RF input from the antenna. The input presents a complex impedance that requires a matching network between the terminal and the antenna. Starting from the substrate (chip) side, the input can be modelled as a lossy capacitor with the bond wire to the ball grid represented as a series inductance.

The terminal is DC blocked. The DC level must not exceed (VSS_RADIO -0.3V to VDD_RADIO + 0.3V).

9.1.3 Transmit RF Power Control for Class 1 Applications (TX_PWR)

An 8-bit voltage DAC (AUX_DAC) is used to control the amplification level of the external PA for Class 1 operation. The DAC output is derived from the on-chip band gap and is virtually independent of temperature and supply voltage. The output voltage is given by:

$$V_{DAC} = MIN\left(\left(3.3v \times \frac{CNTRL\_WORD}{255}\right), (VDD\_PIO - 0.3v)\right)$$

Equation 9.1: Output Voltage with Load Current ≤ 10mA

for a load current ≤10mA (sourced from the device).

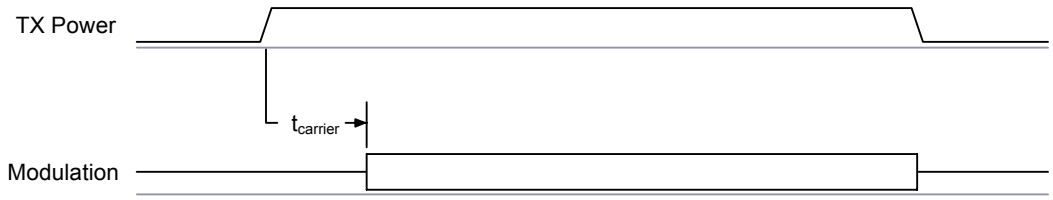
or

$$V_{DAC} = MIN\left(\left(3.3v \times \frac{CNTRL\_WORD}{255}\right), VDD\_PIO\right)$$

Equation 9.2: Output Voltage with No Load Current

for no load current.

BlueCore4-ROM enables the external PA only when transmitting. Before transmitting, the chip normally ramps up the power to the internal PA, then it ramps it down again afterwards. However, if a suitable external PA is used, it may be possible to ramp the power externally by driving the TX_PWR pin on the PA from AUX_DAC.



Equation 9.3: Internal Power Ramping

PSKEY_TX_GAINRAMP (0x1d), is used to control the delay (in units of µs) between the end of the transmit power ramp and the start of modulation. In this period the carrier is transmitted, which gives the transmit circuitry time to fully settle to the correct frequency.

Bits[15:8] define a delay, tcarrier, (in units of µs) between the end of the transmit power ramp and the start of modulation. In this period the carrier is transmitted, which aids interoperability with some other vendor equipment which is not strictly Bluetooth compliant.

9.1.4 Control of External RF Components

TXRX_PIO_CONTROL (0x209) is used to control external RF components such as a switch, an external PA or an external LNA. PIO[0], PIO[1] and the AUX_DAC can be used for this purpose, as Table 9.1 indicates.

TXRX_PIO_CONTROL Value	AUX_DAC Use
0	PIO[0], PIO[1], AUX_DAC not used to control RF. Power ramping is internal.
1	PIO[0] is high during RX, PIO[1] is high during TX. AUX_DAC not used. Power ramping is internal.
2	PIO[0] is high during RX, PIO[1] is high during TX. AUX_DAC used to set gain of external PA. Power ramping is external.
3	PIO[0] is low during RX, PIO[1] is low during TX. AUX_DAC used to set gain of external PA. Power ramping is external.
4	PIO[0] is high during RX, PIO[1] is high during TX. AUX_DAC used to set gain of external PA. Power ramping is internal.

Table 9.1: TXRX_PIO_CONTROL Values

9.2 External Reference Clock Input (XTAL_IN)

The BlueCore4-ROM RF local oscillator and internal digital clocks are derived from the reference clock at the BlueCore4-ROM XTAL_IN input. This reference may be either an external clock or from a crystal connected between XTAL_IN and XTAL_OUT. The crystal mode is described in section 9.3.

9.2.1 External Mode

BlueCore4-ROM can be configured to accept an external reference clock from another device (such as TCXO) at XTAL_IN by connecting XTAL_OUT to ground. The external clock can be either a digital level square wave or sinusoidal, and this may be directly coupled to XTAL_IN without the need for additional components. If the peaks of the reference clock are below VSS_ANA or above VDD_ANA, it must be driven through a DC blocking capacitor (approximately 33pF) connected to XTAL_IN. A digital level reference clock gives superior noise immunity, as the high slew rate clock edges have lower voltage to phase conversion.

The external clock signal should meet the specifications in Table 9.2:

	Min	Typ	Max
Frequency[a]	7.5MHz	16MHz	40MHz
Duty cycle	20:80	50:50	80:20
Edge Jitter (At Zero Crossing)	-	-	15ps rms
Signal Level	400mV pk-pk	-	VDD_ANA[b] [c]

Table 9.2: External Clock Specifications

(a) The frequency should be an integer multiple of 250kHz except for the CDMA/3G frequencies

(b) VDD_ANA is 1.8V nominal

(c) If the external clock is driven through a DC blocking capacitor, then maximum allowable amplitude is reduced from VDD_ANA to 800mV pk-pk

9.2.2 XTAL_IN Impedance in External Mode

The impedance of the XTAL_IN will not change significantly between operating modes, typically 10fF. When transitioning from Deep Sleep to an active state a spike of up to 1pC may be measured. For this reason it is recommended that a buffered clock input be used.

9.2.3 Clock Timing Accuracy

As Figure 9.2 indicates, the 250ppm timing accuracy on the external clock is required 7ms after the assertion of the system clock request line. This is to guarantee that the firmware can maintain timing accuracy in accordance with the Bluetooth v2.0 + EDR specification. Radio activity may occur after 11ms, therefore, at this point the timing accuracy of the external clock source must be within 20ppm.

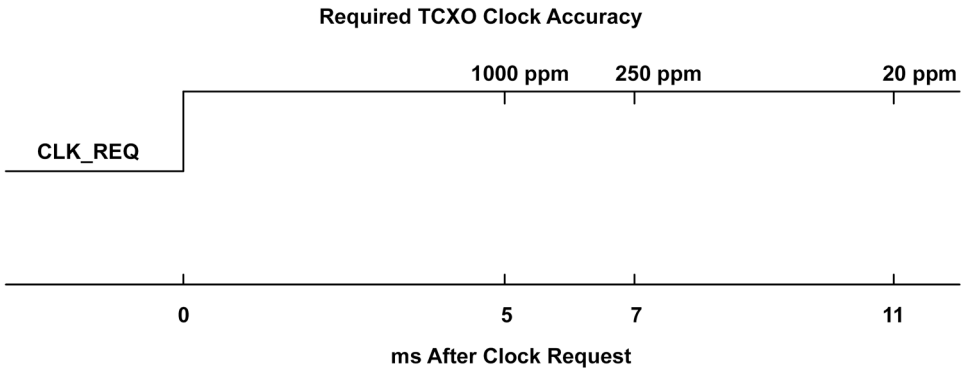


Figure 9.2: TCXO Clock Accuracy

9.2.4 Clock Start-Up Delay

BlueCore4-ROM hardware incorporates an automatic delay after the assertion of the system clock request signal before running firmware. By default, the delay is 5 *low-power oscillator* (LPO) cycles. At a nominal LPO frequency of 1 kHz, this equates to 5 ms. This is suitable for most applications using an external clock source.

However, there may be scenarios where the clock cannot be guaranteed to either exist or be stable after this period. Under these conditions, BlueCore4-ROM provides a function that alters the system clock request signal to the period stored in PSKEY_CLOCK_STARTUP_DELAY. This value is in units of LPO cycles from 1 to 31. Setting the key to zero gives a delay of 5 cycles, the default value.

The nominal frequency of the internal LPO is 1 kHz, however, the value varies somewhat between chips, so care should be taken to pick a suitable value. If an external slow clock at 32 kHz is supplied, this is divided by 32 before use.

This PS Key allows the designer to optimise a system where clock latencies may be longer than 5ms while still keeping the current consumption of BlueCore4-ROM as low as possible. BlueCore4-ROM consumes about 2mA of current for the duration of PSKEY_CLOCK_STARTUP_DELAY before activating the firmware.

9.2.5 Input Frequencies and PS Key Settings

BlueCore4-ROM should be configured to operate with the chosen reference frequency. This is accomplished by setting PSKEY_ANA_FREQ (`0x1fe`) for all frequencies with an integer multiple of 250kHz. The input frequency default setting in BlueCore4-ROM is 26MHz.

The following CDMA/3G TCXO frequencies are also catered for: 7.68, 14.4, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz.

Reference Crystal Frequency (MHz)	PSKEY_ANA_FREQ (0x1fe) (Units of 1kHz)
7.68	7680
14.40	14400
15.36	15360
16.20	16200
16.80	16800
19.20	19200
19.44	19440
19.68	19680
19.80	19800
38.40	38400
n x 250kHz	-
+26.00 Default	26000

Table 9.3: PS Key Values for CDMA/3G Phone TCXO Frequencies

9.3 Crystal Oscillator (XTAL_IN, XTAL_OUT)

This section describes the crystal mode. See section 9.2 for the description of the external reference clock mode.

9.3.1 XTAL Mode

BlueCore4-ROM contains a crystal driver circuit. This operates with an external crystal and capacitors to form a Pierce oscillator.

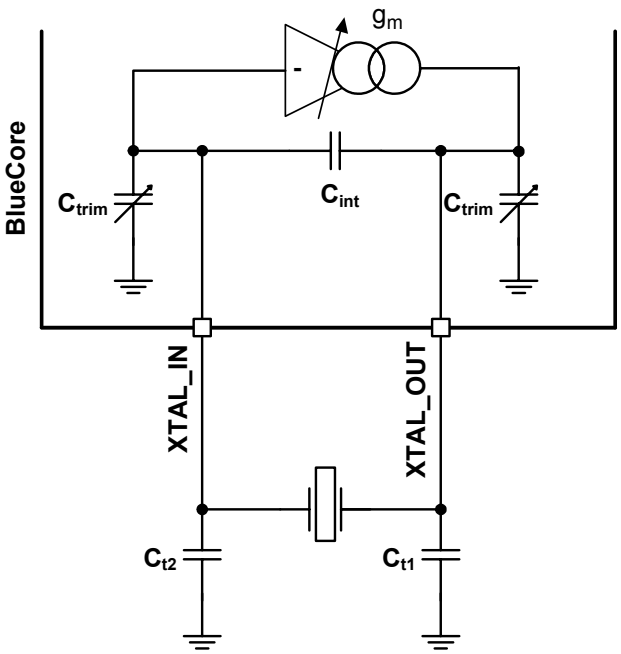


Figure 9.3: Crystal Driver Circuit

Figure 9.4 shows an electrical equivalent circuit for a crystal. The crystal appears inductive near its resonant frequency. It forms a resonant circuit with its load capacitors.

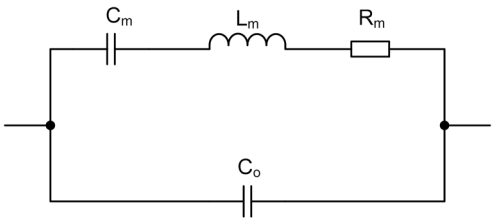


Figure 9.4: Crystal Equivalent Circuit

The resonant frequency may be trimmed with the crystal load capacitance. BlueCore4-ROM contains variable internal capacitors to provide a fine trim.

	Min	Typ	Max
Frequency	8MHz	26MHz	32MHz
Initial Tolerance	-	±25ppm	-
Pullability	-	±20ppm/pF	-

Table 9.4: Crystal Specification

The BlueCore4-ROM driver circuit is a transconductance amplifier. A voltage at XTAL_IN generates a current at XTAL_OUT. The value of transconductance is variable and may be set for optimum performance.

9.3.2 Load Capacitance

For resonance at the correct frequency the crystal should be loaded with its specified load capacitance, which is defined for the crystal. This is the total capacitance across the crystal viewed from its terminals. BlueCore4-ROM provides some of this load with the capacitors C_{trim} and C_{int}. The remainder should be from the external capacitors labelled C_{t1} and C_{t2}. C_{t1} should be three times the value of C_{t2} for best noise performance. This maximises the signal swing, hence, slew rate at XTAL_IN (to which all on-chip clocks are referred). Crystal load capacitance, C_l is calculated with Equation 9.4:

$$C_l = C_{int} + \frac{C_{trim}}{2} + \frac{C_{t1} \bullet C_{t2}}{C_{t1} + C_{t2}}$$

Equation 9.4: Load Capacitance

Where:

C_{trim} = 3.4pF nominal (mid-range setting)

C_{int} = 1.5pF

Note:

C_{int} does not include the crystal internal self capacitance; it is the driver self capacitance.

9.3.3 Frequency Trim

BlueCore4-ROM enables frequency adjustments to be made. This feature is typically used to remove initial tolerance frequency errors associated with the crystal. Frequency trim is achieved by adjusting the crystal load capacitance with on-chip trim capacitors, C_{trim}. The value of C_{trim} is set by a 6-bit word in PSKEY_ANA_FTRIM (0x1f6). Its value is calculated thus:

$$C_{trim} = 110fF \times PSKEY\_ANA\_FTRIM$$

Equation 9.5: Trim Capacitance

There are two C_{trim} capacitors, which are both connected to ground. When viewed from the crystal terminals, they appear in series so each least significant bit (LSB) increment of frequency trim presents a load across the crystal of 55fF.

The frequency trim is described by Equation 9.6.

$$\frac{\Delta(F_X)}{F_X} = pullability \times 55 \times 10^{-3} (ppm/LSB)$$

Equation 9.6: Frequency Trim

Where Fx is the crystal frequency and pullability is a crystal parameter with units of ppm/pF. Total trim range is 63 times the value above.

If not specified, the pullability of a crystal may be calculated from its motional capacitance with Equation 9.7.

$$\frac{\partial(F_X)}{\partial(C)} = F_X \cdot \frac{C_m}{2(C_l + C_0)^2}$$

Equation 9.7: Pullability

Where:

C_0 = Crystal self capacitance (shunt capacitance)

C_m = Crystal motional capacitance (series branch capacitance in crystal model). See Figure 9.4.

Note:

It is a Bluetooth requirement that the frequency is always within ±20ppm. The trim range should be sufficient to pull the crystal within ±5ppm of the exact frequency. This leaves a margin of ±15ppm for frequency drift with ageing and temperature. A crystal with an ageing and temperature drift specification of better than ±15ppm is required.

9.3.4 Transconductance Driver Model

The crystal and its load capacitors should be viewed as a transimpedance element, whereby a current applied to one terminal generates a voltage at the other. The transconductance amplifier in BlueCore4-ROM uses the voltage at its input, XTAL_IN, to generate a current at its output, XTAL_OUT. Therefore, the circuit will oscillate if the transconductance, transimpedance product is greater than unity. For sufficient oscillation amplitude, the product should be greater than three. The transconductance required for oscillation is defined by the relationship shown in Equation 9.8:

$$g_m > \frac{3(2\pi F_x)^2 R_m((C_0 + C_{int})(C_{t1} + C_{t2} + C_{trim}) + (C_{t1} + C_{trim})(C_{t2} + C_{trim}))^2}{(C_{t1} + C_{trim})(C_{t2} + C_{trim})}$$

Equation 9.8: Transconductance Required for Oscillation

BlueCore4-ROM guarantees a transconductance value of at least 2mA/V at maximum drive level.

Notes:

More drive strength is required for higher frequency crystals, higher loss crystals (larger R_m) or higher capacitance loading.

Optimum drive level is attained when the level at XTAL_IN is approximately 1V pk-pk. The drive level is determined by the crystal driver transconductance, by setting PSKEY_XTAL_LVL (`0x241`).

9.3.5 Negative Resistance Model

An alternative representation of the crystal and its load capacitors is a frequency dependent resistive element. The driver amplifier may be considered as a circuit that provides negative resistance. For oscillation, the value of the negative resistance must be greater than that of the crystal circuit equivalent resistance. Although the BlueCore4-ROM crystal driver circuit is based on a transimpedance amplifier, an equivalent negative resistance may be calculated for it with the following formula in Equation 9.9:

$$R_{neg} > \frac{(C_{t1} + C_{trim})(C_{t2} + C_{trim})}{g_m(2\pi F_X)^2((C_0 + C_{int})(C_{t1} + C_{t2} + 2C_{trim}) + (C_{t1} + C_{trim})(C_{t2} + C_{trim}))^2}$$

Equation 9.9: Equivalent Negative Resistance

This formula shows the negative resistance of the BlueCore4-ROM driver as a function of its drive strength.

The value of the driver negative resistance may be easily measured by placing an additional resistance in series with the crystal. The maximum value of this resistor (oscillation occurs) is the equivalent negative resistance of the oscillator.

9.3.6 Crystal PS Key Settings

See tables in section 9.2.5.

9.3.7 Crystal Oscillator Characteristics

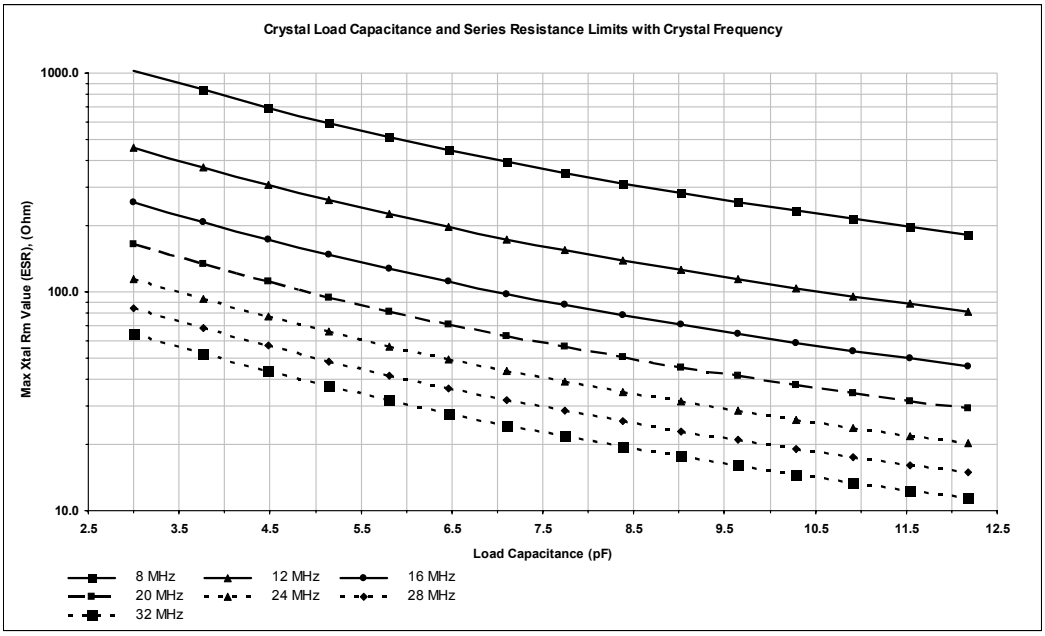


Figure 9.5: Crystal Load Capacitance and Series Resistance Limits with Crystal Frequency

Note:

Graph shows results for BlueCore4-ROM crystal driver at maximum drive level.

Conditions:

C_{trim} = 3.4pF centre value

Crystal C_o = 2pF

Transconductance setting = 2mA/V

Loop gain = 3

C_{t1}/C_{t2} = 3

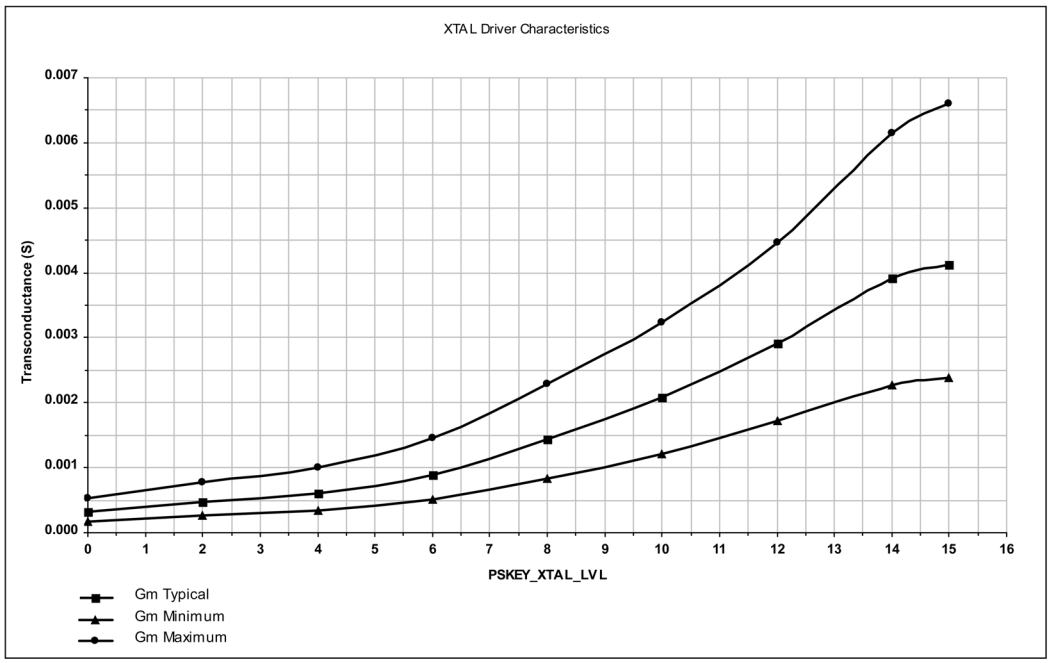


Figure 9.6: Crystal Driver Transconductance vs. Driver Level Register Setting

Note:

Drive level is set by PSKEY_XTAL_LVL (`0x241`).

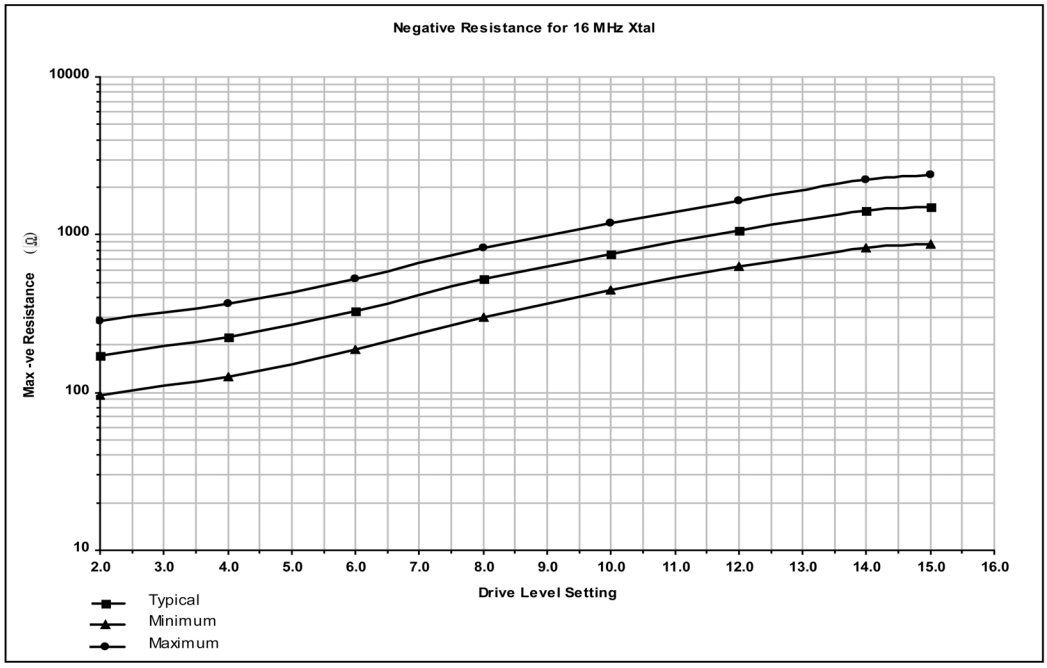


Figure 9.7: Crystal Driver Negative Resistance as a Function of Drive Level Setting

Crystal parameters:

Crystal frequency 16MHz (refer to your software build release note for supported frequencies).

Crystal C_0 = 0.75pF

Circuit parameters:

C_{trim} = 8pF, maximum value

C_{t1},C_{t2} = 5pF (3.9pF plus 1.1 pF stray)

(Crystal total load capacitance 8.5pF)

Note:

This is for a specific crystal and load capacitance.

9.4 UART Interface

This is a standard *Universal Asynchronous Receiver Transmitter* (UART) interface for communicating with other serial devices.

BlueCore4-ROM UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.(1)

(1) Uses RS232 protocol, but voltage levels are 0V to VDD_USB (requires external RS232 transceiver chip).

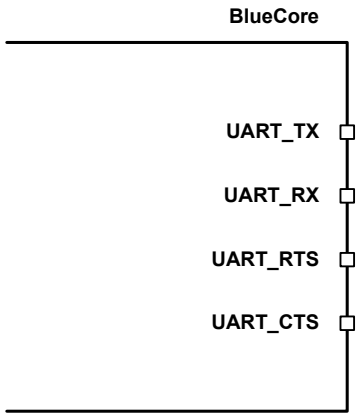


Figure 9.8: Universal Asynchronous Receiver

Four signals are used to implement the UART function, as shown in Figure 9.8. When BlueCore4-ROM is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators. All UART connections are implemented using CMOS technology and have signalling levels of 0V and VDD_USB.

UART configuration parameters, such as data rate and packet format, are set using BlueCore4-ROM software.

Note:

In order to communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

Parameter		Possible Values
Data Rate	Minimum	1200 bits/s (≤2%Error)
		9600 bits/s (≤1%Error)
	Maximum	3M bit/s (≤1%Error)
Flow Control		RTS/CTS or None
Parity		None, Odd or Even
Number of Stop Bits		1 or 2
Bits per Channel		8

Table 9.5: Possible UART Settings

The UART interface is capable of resetting BlueCore4-ROM upon reception of a break signal. A break is identified by a continuous logic low (0V) on the UART_RX terminal, as shown in Figure 9.9. If t_{BRK} is longer than the value, defined by PSKEY_HOST_IO_UART_RESET_TIMEOUT, (`0x1a4`), a reset will occur. This feature allows a host to initialise the system to a known state. Also, BlueCore4-ROM can emit a break character that may be used to wake the host.

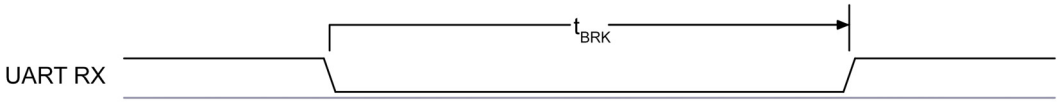


Figure 9.9: Break Signal

Note:

The DFU boot loader must be loaded into the Flash device before the UART or USB interfaces can be used. This initial flash programming can be done via the SPI.

Table 9.6 shows a list of commonly used data rates and their associated values for PSKEY_UART_BAUD_RATE (0x204). There is no requirement to use these standard values. Any data rate within the supported range can be set in the PS Key according to the formula in Equation 9.10.

$$\text{Data Rate} = \frac{\text{PSKEY\_UART\_BAUDRATE}}{0.004096}$$

Equation 9.10: Data Rate

Data Rate (bits/s)	Persistent Store Value		Error
	Hex	Dec	
1200	0x0005	5	1.73%
2400	0x000a	10	1.73%
4800	0x0014	20	1.73%
9600	0x0027	39	-0.82%
19200	0x004f	79	0.45%
38400	0x009d	157	-0.18%
57600	0x00ec	236	0.03%
76800	0x013b	315	0.14%
115200	0x01d8	472	0.03%
230400	0x03b0	944	0.03%
460800	0x075f	1887	-0.02%
921600	0x0ebf	3775	0.00%
1382400	0x161e	5662	-0.01%
1843200	0x1d7e	7550	0.00%
2764800	0x2c3d	11325	0.00%

Table 9.6: Standard Data Rates

9.4.1 UART Bypass

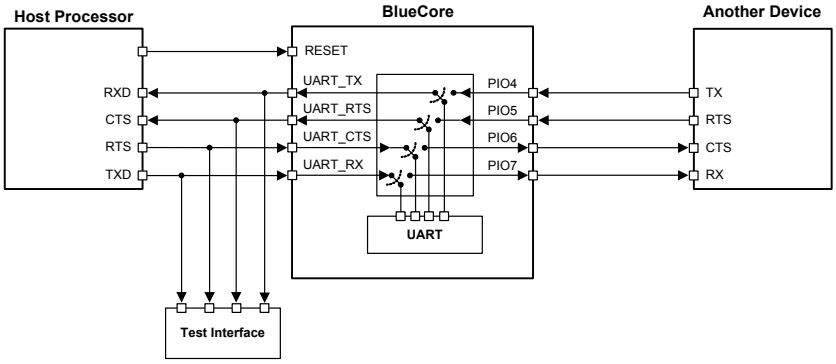


Figure 9.10: UART Bypass Architecture

9.4.2 UART Configuration While RESET is Active

The UART interface for BlueCore4-ROM while the chip is being held in reset is tri-state. This will allow the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tri-state when BlueCore4-ROM reset is de-asserted and the firmware begins to run.

9.4.3 UART Bypass Mode

Alternatively, for devices that do not tri-state the UART bus, the UART bypass mode on BlueCore4-ROM can be used. The default state of BlueCore4-ROM after reset is de-asserted; this is for the host UART bus to be connected to the BlueCore4-ROM UART, thereby allowing communication to BlueCore4-ROM via the UART. All UART bypass mode connections are implemented using CMOS technology and have signalling levels of 0V and VDD_PADS.(1)

In order to apply the UART bypass mode, a BCCMD command will be issued to BlueCore4-ROM. Upon this issue, it will switch the bypass to PIO[7:4] as Figure 9.10 indicates. Once the bypass mode has been invoked, BlueCore4-ROM will enter the Deep Sleep state indefinitely.

In order to re-establish communication with BlueCore4-ROM, the chip must be reset so that the default configuration takes effect.

It is important for the host to ensure a clean Bluetooth disconnection of any active links before the bypass mode is invoked. Therefore, it is not possible to have active Bluetooth links while operating the bypass mode.

9.4.4 Current Consumption in UART Bypass Mode

The current consumption for a device in UART bypass mode is equal to the values quoted for a device in standby mode.

9.5 USB Interface

This is a full speed (12Mbits/s) *Universal Serial Bus* (USB) interface for communicating with other compatible digital devices. BlueCore4-ROM acts as a USB peripheral, responding to requests from a master host controller such as a PC.

The USB interface is capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported. The set of USB endpoints implemented can behave as specified in the USB section of the Bluetooth specification v2.1 + EDR or alternatively can appear as a set of endpoints appropriate to USB audio devices such as speakers.

As USB is a master/slave oriented system (in common with other USB peripherals), BlueCore4-ROM only supports USB Slave operation.

(1) The range of the signalling level for the standard UART described in section 9.4 and the UART bypass may differ between CSR BlueCore devices, as the power supply configurations are chip dependent. For BlueCore4-ROM, the standard UART is supplied by VDD_USB, so has signalling levels of 0V and VDD_USB. Whereas in the UART bypass mode, the signals appear on PIO[4:7] which are supplied by VDD_PADS, therefore the signalling levels are 0V and VDD_PADS.

9.5.1 USB Data Connections

The USB data lines emerge as pins USB_DP and USB_DN. These terminals are connected to the internal USB I/O buffers of the BlueCore4-ROM, therefore, have a low output impedance. To match the connection to the characteristic impedance of the USB cable, resistors must be placed in series with USB_DP/USB_DN and the cable.

9.5.2 USB Pull-Up Resistor

BlueCore4-ROM features an internal USB pull-up resistor. This pulls the USB_DP pin weakly high when BlueCore4-ROM is ready to enumerate. It signals to the PC that it is a full speed (12Mbits/s) USB device.

The USB internal pull-up is implemented as a current source, and is compliant with section 7.1.5 of the USB specification v1.2. The internal pull-up pulls USB_DP high to at least 2.8V when loaded with a 15kΩ ±5% pull-down resistor (in the hub/host) when VDD_PADS = 3.1V. This presents a Thevenin resistance to the host of at least 900Ω. Alternatively, an external 1.5kΩ pull-up resistor can be placed between a PIO line and D+ on the USB cable. The firmware must be alerted to which mode is used by setting PSKEY_USB_PIO_PULLUP appropriately. The default setting uses the internal pull-up resistor.

9.5.3 USB Power Supply

The USB specification dictates that the minimum output high voltage for USB data lines is 2.8V. To safely meet the USB specification, the voltage on the VDD_USB supply terminals must be an absolute minimum of 3.1V. CSR recommends 3.3V for optimal USB signal quality.

9.5.4 Self-Powered Mode

In self-powered mode, the circuit is powered from its own power supply and not from the VBUS (5V) line of the USB cable. It draws only a small leakage current (below 0.5mA) from VBUS on the USB cable. This is the easier mode for which to design, as the design is not limited by the power that can be drawn from the USB hub or root port. However, it requires that VBUS be connected to BlueCore4-ROM via a resistor network (R_{vb1} and R_{vb2}), so BlueCore4-ROM can detect when VBUS is powered up. BlueCore4-ROM will not pull USB_DP high when VBUS is off.

Self-powered USB designs (powered from a battery or PSU) must ensure that a PIO line is allocated for USB pull-up purposes. A 1.5kΩ 5% pull-up resistor between USB_DP and the selected PIO line should be fitted to the design. Failure to fit this resistor may result in the design failing to be USB compliant in self-powered mode. The internal pull-up in BlueCore is only suitable for bus-powered USB devices, e.g., dongles.

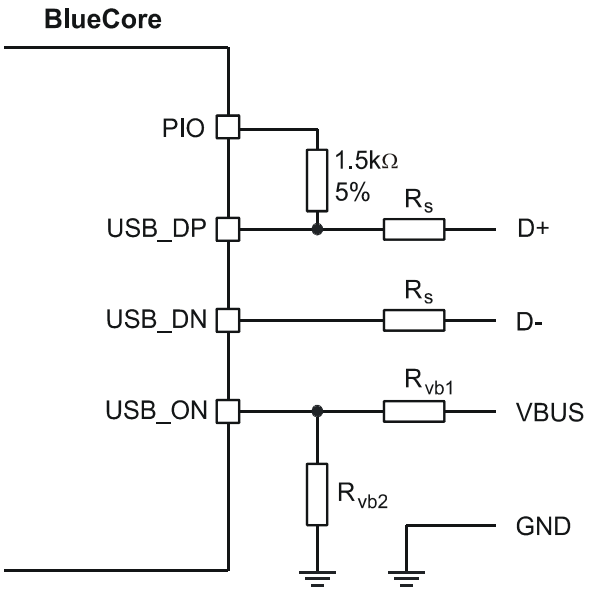


Figure 9.11: USB Connections for Self-Powered Mode

The terminal marked USB_ON can be any free PIO pin. The PIO pin selected must be registered by setting PSKEY_USB_PIO_VBUS to the corresponding pin number.

Note:

USB_ON is shared with BlueCore4-ROM PIO terminals.

Identifier	Value	Function
R_s	27Ω nominal	Impedance matching to USB cable
R_{vb1}	22kΩ 5%	VBUS ON sense divider
R_{vb2}	47kΩ 5%	VBUS ON sense divider

Table 9.7: USB Interface Component Values

9.5.5 Bus-Powered Mode

In bus-powered mode, the application circuit draws its current from the 5V VBUS supply on the USB cable. BlueCore4-ROM negotiates with the PC during the USB enumeration stage about how much current it is allowed to consume.

For Class 2 Bluetooth applications, CSR recommends that the regulator used to derive 3.3V from VBUS is rated at 100mA average current and should be able to handle peaks of 120mA without foldback or limiting. In bus-powered mode, BlueCore4-ROM requests 100mA during enumeration.

For Class 1 Bluetooth applications, the USB power descriptor should be altered to reflect the amount of power required. This is accomplished by setting PSKEY_USB_MAX_POWER (0x2c6). This is higher than for a Class 2 application due to the extra current drawn by the Transmit RF PA.

When selecting a regulator, be aware that VBUS may go as low as 4.4V. The inrush current (when charging reservoir and supply decoupling capacitors) is limited by the USB specification. See USB Specification v1.1, section 7.2.4.1. Some applications may require soft start circuitry to limit inrush current if more than 10µF is present between VBUS and GND.

The 5V VBUS line emerging from a PC is often electrically noisy. As well as regulation down to 3.3V and 1.8V, applications should include careful filtering of the 5V line to attenuate noise that is above the voltage regulator bandwidth. Excessive noise on the 1.8V supply to the analogue supply pins of BlueCore4-ROM will result in reduced receive sensitivity and a distorted RF transmit signal.

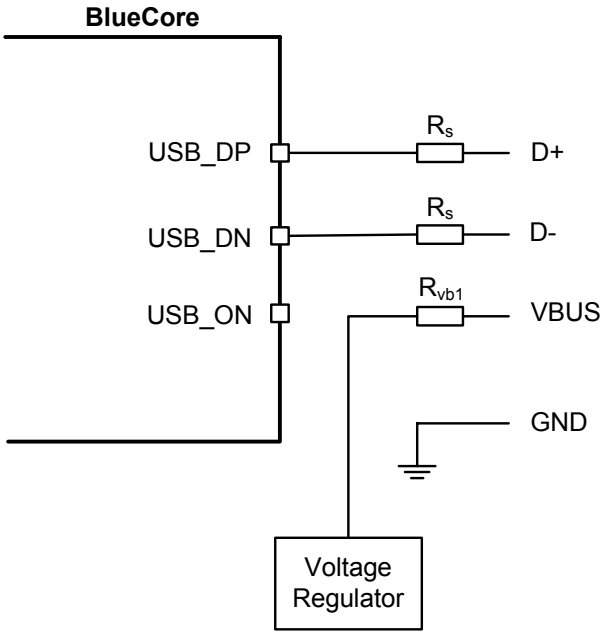


Figure 9.12: USB Connections for Bus-Powered Mode

9.5.6 Suspend Current

All USB devices must permit the USB controller to place them in a USB suspend mode. While in USB Suspend, bus-powered devices must not draw more than 0.5mA from USB VBUS (self-powered devices may draw more than 0.5mA from their own supply). This current draw requirement prevents operation of the radio by bus-powered devices during USB Suspend.

The voltage regulator circuit itself should draw only a small quiescent current (typically less than 100µA) to ensure adherence to the suspend current requirement of the USB specification. This is not normally a problem with modern regulators. Ensure that external LEDs and/or amplifiers can be turned off by BlueCore4-ROM. The entire circuit must be able to enter the suspend mode. Refer to separate CSR documentation for more details on USB Suspend.

9.5.7 Detach and Wake_Up Signalling

BlueCore4-ROM can provide out-of-band signalling to a host controller by using the control lines called USB_DETACH and USB_WAKE_UP. These are outside the USB specification (no wires exist for them inside the USB cable), but can be useful when embedding BlueCore4-ROM into a circuit where no external USB is visible to the user. Both control lines are shared with PIO pins and can be assigned to any PIO pin by setting PSKEY_USB_PIO_DETACH and PSKEY_USB_PIO_WAKEUP to the selected PIO number.

USB_DETACH is an input which, when asserted high, causes BlueCore4-ROM to put USB_DN and USB_DP in a high impedance state and turns off the pull-up resistor on DP. This detaches the device from the bus and is logically equivalent to unplugging the device. When USB_DETACH is taken low, BlueCore4-ROM will connect back to USB and await enumeration by the USB host.

USB_WAKE_UP is an active high output (used only when USB_DETACH is active) to wake up the host and allow USB communication to recommence. It replaces the function of the software USB WAKE_UP message (which runs over the USB cable) and cannot be sent while BlueCore4-ROM is effectively disconnected from the bus.

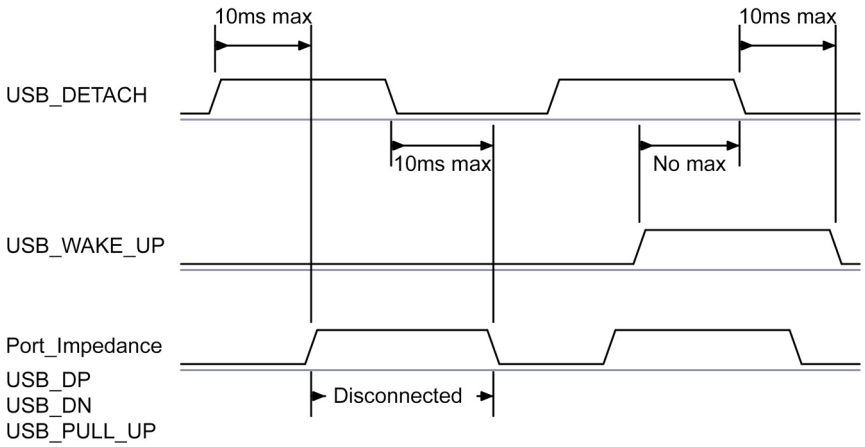


Figure 9.13: USB_DETACH and USB_WAKE_UP Signal

9.5.8 USB Driver

A USB Bluetooth device driver is required to provide a software interface between BlueCore4-ROM and Bluetooth software running on the host computer. Suitable drivers are available from http://www.csrsupport.com.

9.5.9 USB 1.1 Compliance

BlueCore4-ROM is qualified to the *USB Specification v1.1*, details of which are available from http://www.usb.org. The specification contains valuable information on aspects such as PCB track impedance, supply inrush current and product labelling.

Although BlueCore4-ROM meets the USB specification, CSR cannot guarantee that an application circuit designed around the chip is USB compliant. The choice of application circuit, component choice and PCB layout all affect USB signal quality and electrical characteristics. The information in this document is intended as a guide and should be read in association with the USB specification, with particular attention being given to Chapter 7. Independent USB qualification must be sought before an application is deemed USB compliant and can bear the USB logo. Such qualification can be obtained from a USB plugfest or from an independent USB test house.

Terminals USB_DP and USB_DN adhere to the *USB Specification v2.0 (Chapter 7)* electrical requirements.

9.5.10 USB 2.0 Compatibility

BlueCore4-ROM is compatible with USB v2.0 host controllers; under these circumstances the two ends agree the mutually acceptable rate of 12Mbits/s according to the USB v2.0 specification.

9.6 Serial Peripheral Interface

BlueCore4-ROM uses 16-bit data and 16-bit address serial peripheral interface, where transactions may occur when the internal processor is running or is stopped. This section details the considerations required when interfacing to BlueCore4-ROM via the four dedicated serial peripheral interface terminals. Data may be written or read one word at a time or the auto increment feature may be used to access blocks.

9.6.1 Instruction Cycle

The BlueCore4-ROM is the slave and receives commands on SPI_MOSI and outputs data on SPI_MISO. Table 9.8 shows the instruction cycle for an SPI transaction.

1	Reset the SPI interface	Hold SPI_CSB high for two SPI_CLK cycles
2	Write the command word	Take SPI_CSB low and clock in the 8 bit command
3	Write the address	Clock in the 16-bit address word
4	Write or read data words	Clock in or out 16-bit data word(s)
5	Termination	Take SPI_CSB high

Table 9.8: Instruction Cycle for an SPI Transaction

With the exception of reset,SPI_CSB must be held low during the transaction. Data on SPI_MOSI is clocked into the BlueCore4-ROM on the rising edge of the clock line SPI_CLK. When reading, BlueCore4-ROM will reply to the master on SPI_MISO with the data changing on the falling edge of the SPI_CLK. The master provides the clock on SPI_CLK. The transaction is terminated by taking SPI_CSB high.

Sending a command word and the address of a register for every time it is to be read or written is a significant overhead, especially when large amounts of data are to be transferred. To overcome this BlueCore4-ROM offers increased data transfer efficiency via an auto increment operation. To invoke auto increment, SPI_CSB is kept low, which auto increments the address, while providing an extra 16 clock cycles for each extra word to be written or read.

9.6.2 Writing to the Device

To write to BlueCore4-ROM, the 8-bit write command (00000010) is sent first (C[7:0]) followed by a 16-bit address (A[15:0]). The next 16-bits (D[15:0]) clocked in on SPI_MOSI are written to the location set by the address (A). Thereafter for each subsequent 16-bits clocked in, the address (A) is incremented and the data written to consecutive locations until the transaction terminates when SPI_CSB is taken high.

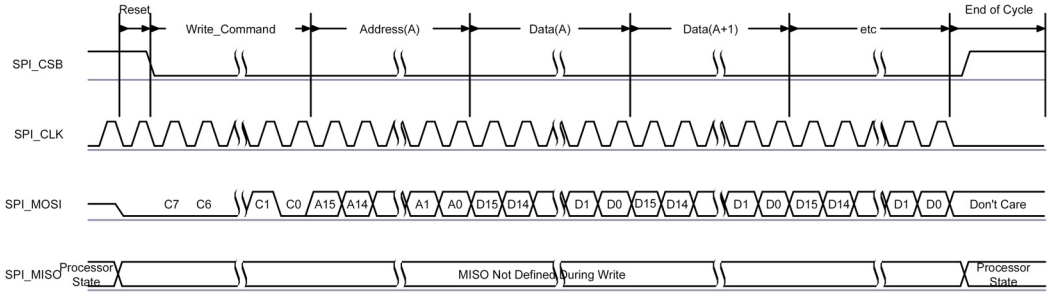


Figure 9.14: SPI Write Operation

9.6.3 Reading from the Device

Reading from BlueCore4-ROM is similar to writing to it. An 8-bit read command (00000011) is sent first (C[7:0]), followed by the address of the location to be read (A[15:0]).BlueCore4-ROM then outputs on SPI_MISO a check word during T[15:0] followed by the 16-bit contents of the addressed location during bits D[15:0].

The check word is composed of {command, address [15:8]}. The check word may be used to confirm a read operation to a memory location. This overcomes the problems encountered with typical serial peripheral interface slaves, whereby it is impossible to determine whether the data returned by a read operation is valid data or the result of the slave device not responding.

If SPI_CSB is kept low, data from consecutive locations is read out on SPI_MISO for each subsequent 16 clocks, until the transaction terminates when SPI_CSB is taken high.

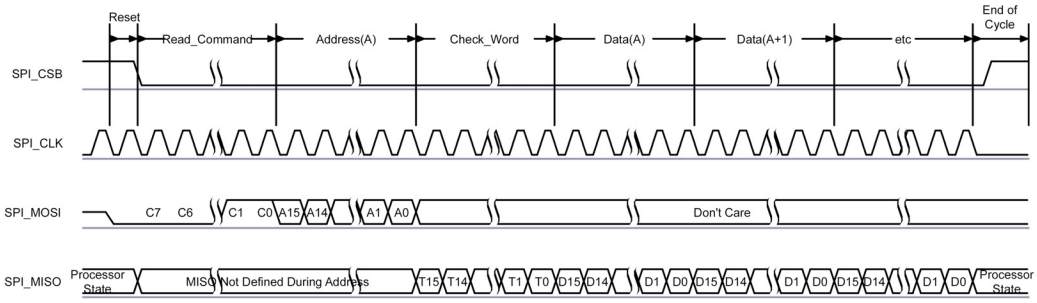


Figure 9.15: SPI Read Operation

9.6.4 Multi-Slave Operation

BlueCore4-ROM should not be connected in a multi-slave arrangement by simple parallel connection of slave MISO lines. When BlueCore4-ROM is deselected (SPI_CSB = 1), the SPI_MISO line does not float. Instead, BlueCore4-ROM outputs 0 if the processor is running or 1 if it is stopped.

9.7 PCM CODEC Interface

Pulse Code Modulation (PCM) is a standard method used to digitise audio (particularly voice) for transmission over digital communication channels. Through its PCM interface, BlueCore4-ROM has hardware support for continual transmission and reception of PCM data, thus reducing processor overhead for wireless headset applications. BlueCore4-ROM offers a bi-directional digital audio interface that routes directly into the baseband layer of the on-chip firmware. It does not pass through the HCI protocol layer.

Hardware on BlueCore4-ROM allows the data to be sent to and received from a SCO connection. (1)

Up to three SCO connections can be supported by the PCM interface at any one time.

BlueCore4-ROM can operate as the PCM interface master generating an output clock of 128, 256 or 512kHz. When configured as PCM interface slave, it can operate with an input clock up to 2048kHz. BlueCore4-ROM is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13-bit or 16-bit linear, 8-bit μ-law or A-law companded sample formats at 8ksamples/s and can receive and transmit on any selection of three of the first four slots following PCM_SYNC. The PCM configuration options are enabled by setting PSKEY_PCM_CONFIG32 (`0x1b3`).

BlueCore4-ROM interfaces directly to PCM audio devices including the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 four channel A-law and μ-law CODEC
- Motorola MC145481 8-bit A-law and μ-law CODEC
- Motorola MC145483 13-bit linear CODEC
- STW 5093 and 5094 14-bit linear CODECs
- BlueCore4-ROM is also compatible with the Motorola SSI interface

9.7.1 PCM Interface Master/Slave

When configured as the master of the PCM interface, BlueCore4-ROM generates PCM_CLK and PCM_SYNC.

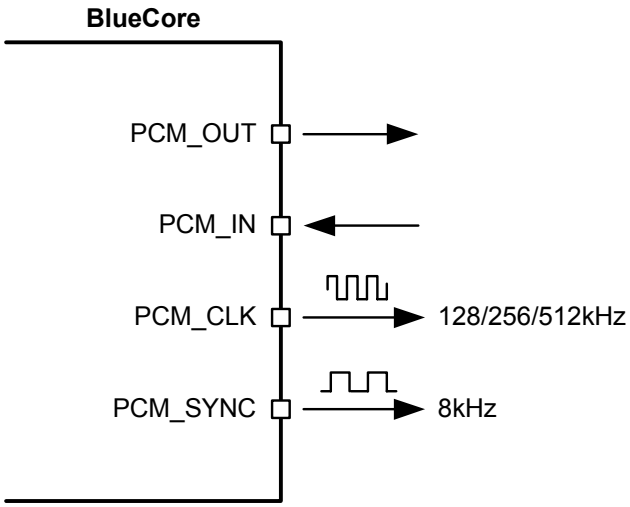


Figure 9.16: BlueCore4-ROM as PCM Interface Master

When configured as the Slave of the PCM interface, BlueCore4-ROM accepts PCM_CLK rates up to 2048kHz.

(1) Subject to firmware support. Contact CSR for current status.

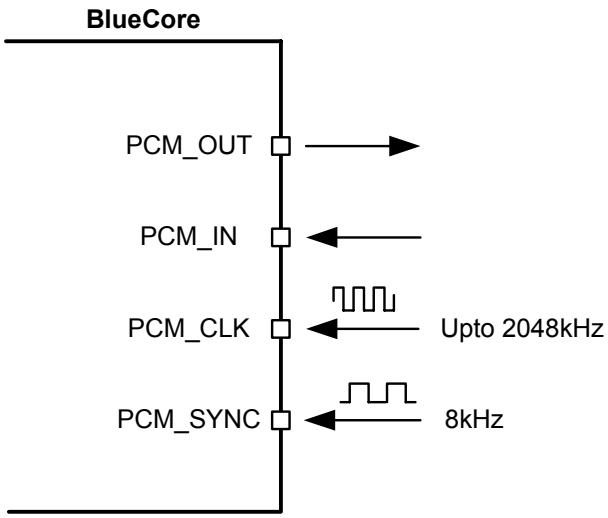


Figure 9.17: BlueCore4-ROM as PCM Interface Slave

9.7.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When BlueCore4-ROM is configured as PCM master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8-bits long. When BlueCore4-ROM is configured as PCM Slave, PCM_SYNC may be from two consecutive falling edges of PCM_CLK to half the PCM_SYNC rate, i.e., 62.5µs long.

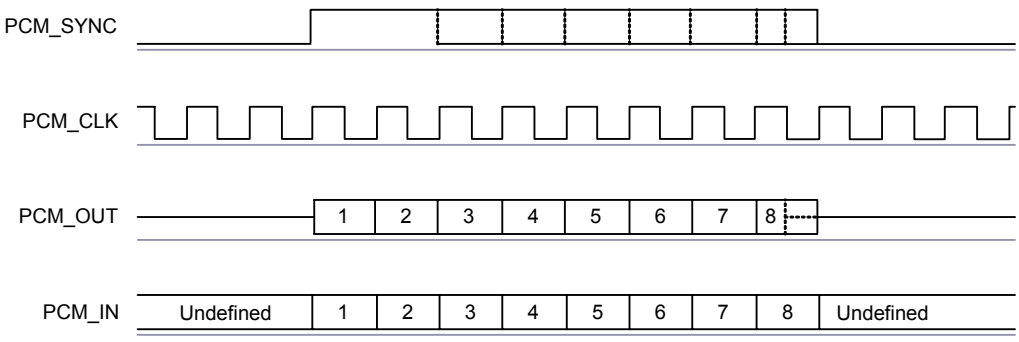


Figure 9.18: Long Frame Sync (Shown with 8-bit Companded Sample)

BlueCore4-ROM samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

9.7.3 Short Frame Sync

In Short Frame Sync, the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

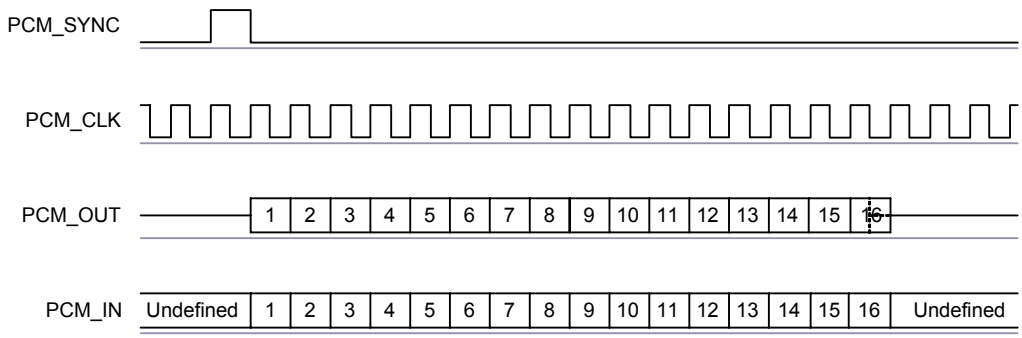


Figure 9.19: Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, BlueCore4-ROM samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

9.7.4 Multi-slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections can be carried over any of the first four slots.

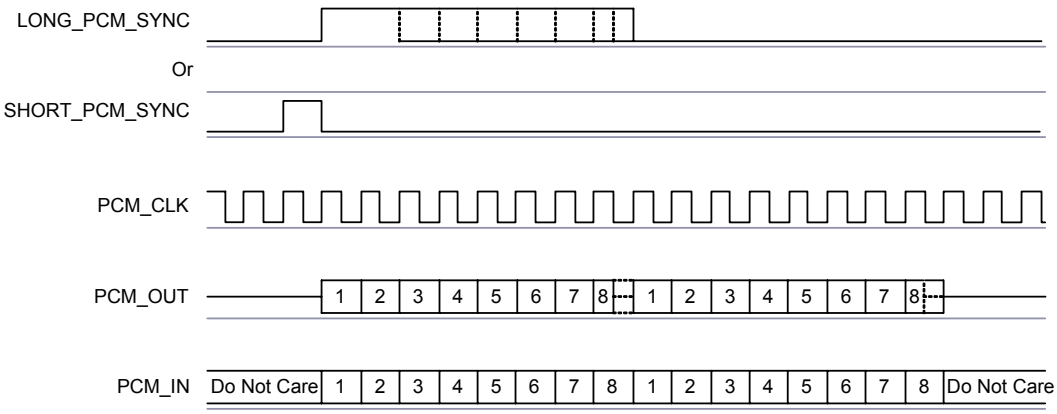


Figure 9.20: Multi-slot Operation with Two Slots and 8-bit Companded Samples

9.7.5 GCI Interface

BlueCore4-ROM is compatible with the *General Circuit Interface* (GCI), a standard synchronous 2B+D ISDN timing interface. The two 64kbits/s B channels can be accessed when this mode is configured.

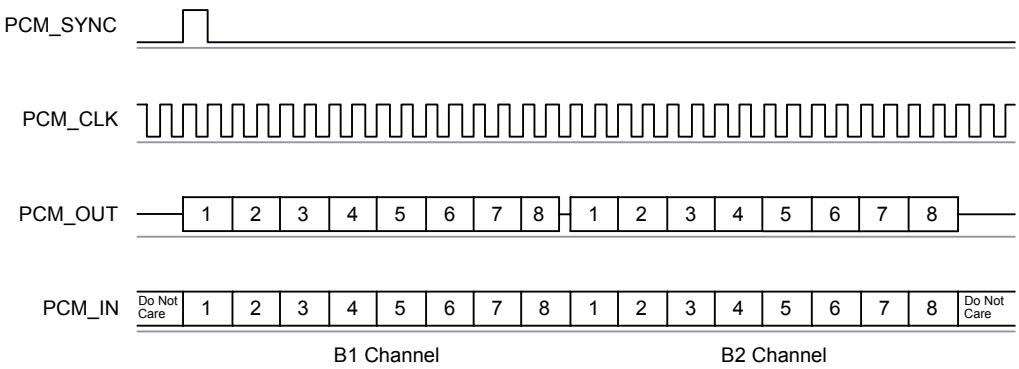


Figure 9.21: GCI Interface

The start of frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz. With BlueCore4-ROM in Slave mode, the frequency of PCM_CLK can be up to 4.096MHz.

9.7.6 Slots and Sample Formats

BlueCore4-ROM can receive and transmit on any selection of the first four slots following each sync pulse. Slot durations can be either 8 or 16 clock cycles. Durations of 8 clock cycles may only be used with 8-bit sample formats. Durations of 16 clocks may be used with 8-bit, 13-bit or 16-bit sample formats.

BlueCore4-ROM supports 13-bit linear, 16-bit linear and 8-bit μ-law or A-law sample formats. The sample rate is 8ksamples/s. The bit order may be little or big endian. When 16-bit slots are used, the 3 or 8 unused bits in each slot may be filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some Motorola CODECs.

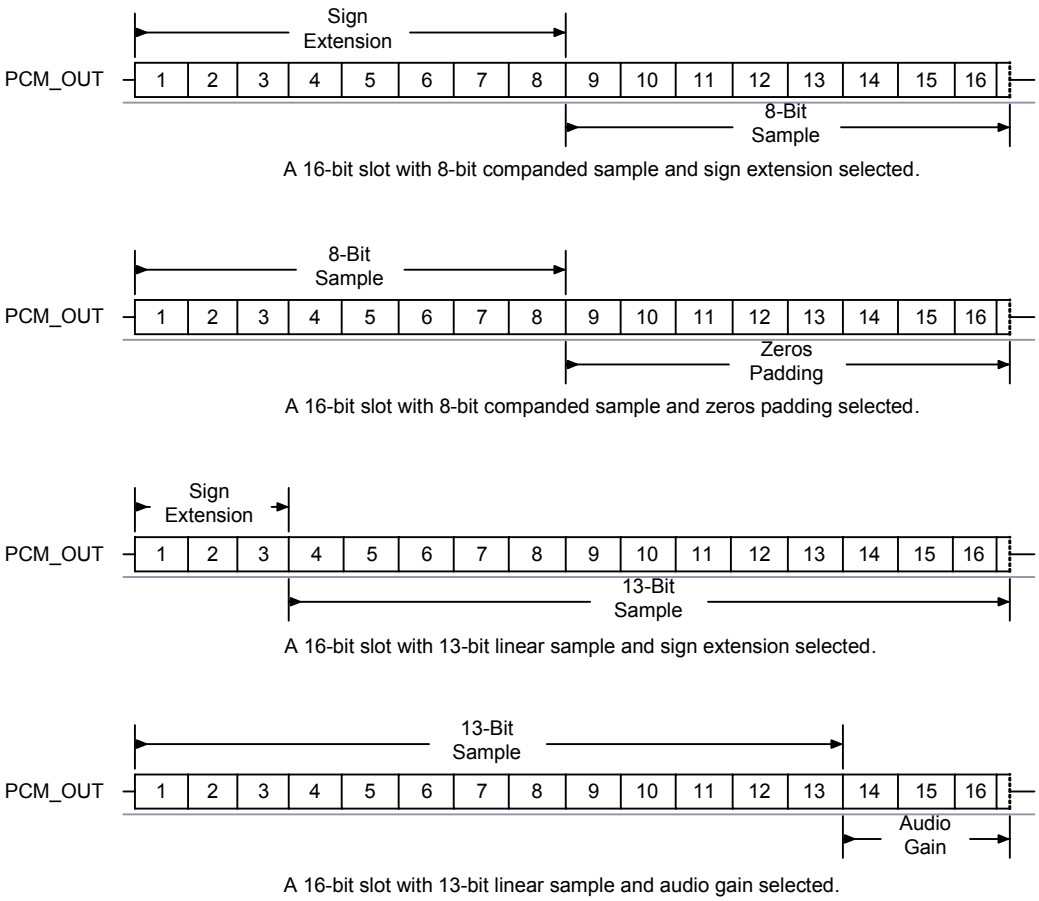


Figure 9.22: 16-Bit Slot Length and Sample Formats

9.7.7 Additional Features

BlueCore4-ROM has a mute facility that forces PCM_OUT to be 0. In master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running which some CODECs use to control power down.

9.7.8 PCM Timing Information

Symbol	Parameter		Min	Typ	Max	Unit
f_{mclk}	PCM_CLK frequency	4MHz DDS generation. Selection of frequency is programmable. See Table 9.11.	-	128 256 512	-	kHz
		48MHz DDS generation. Selection of frequency is programmable. See Table 9.12 and PCM_CLK and PCM_SYNC Generation on page 79.	2.9		-	kHz
-	PCM_SYNC frequency		-	8		kHz
t_{mclkh}[(a)]	PCM_CLK high	4MHz DDS generation	980	-	-	ns
t_{mclkl}[(a)]	PCM_CLK low	4MHz DDS generation	730	-		ns
-	PCM_CLK jitter	48MHz DDS generation			21	ns pk-pk
$t_{dmclksynch}$	Delay time from PCM_CLK high to PCM_SYNC high		-	-	20	ns
$t_{dmclkpout}$	Delay time from PCM_CLK high to valid PCM_OUT		-	-	20	ns
$t_{dmclklsyncl}$	Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only)		-	-	20	ns
$t_{dmclkhsyncl}$	Delay time from PCM_CLK high to PCM_SYNC low		-	-	20	ns
$t_{dmclklpoutz}$	Delay time from PCM_CLK low to PCM_OUT high impedance		-	-	20	ns
$t_{dmclkhpoutz}$	Delay time from PCM_CLK high to PCM_OUT high impedance		-	-	20	ns
$t_{supinclkl}$	Set-up time for PCM_IN valid to PCM_CLK low		30	-	-	ns
$t_{hpinclkl}$	Hold time for PCM_CLK low to PCM_IN invalid		10	-	-	ns

Table 9.9: PCM Master Timing

(a) Assumes normal system clock operation. Figures will vary during low power modes, when system clock speeds are reduced.

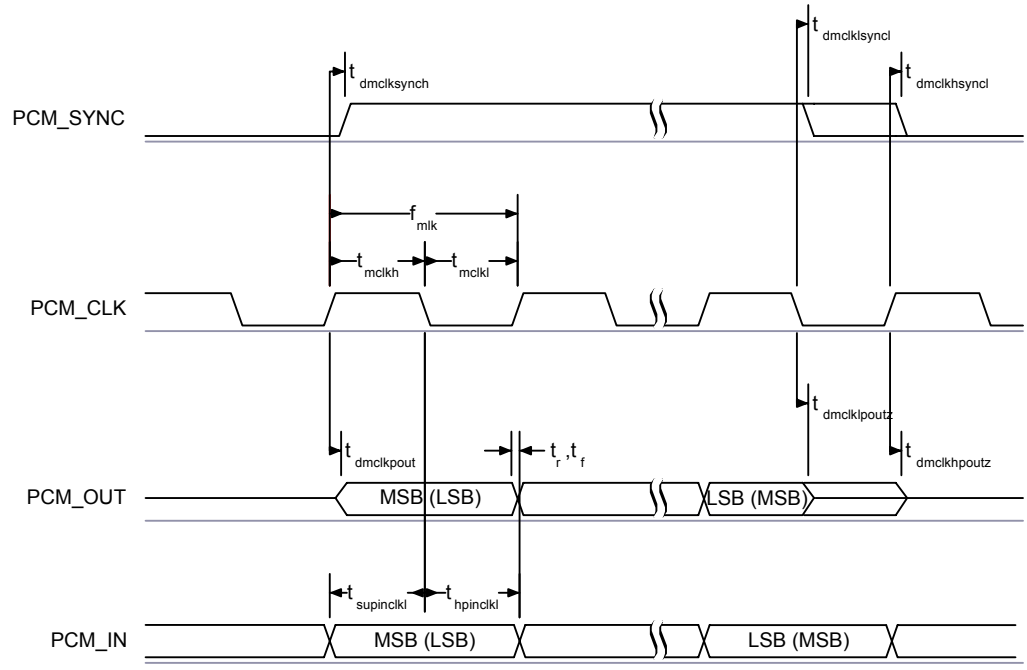


Figure 9.23: PCM Master Timing Long Frame Sync

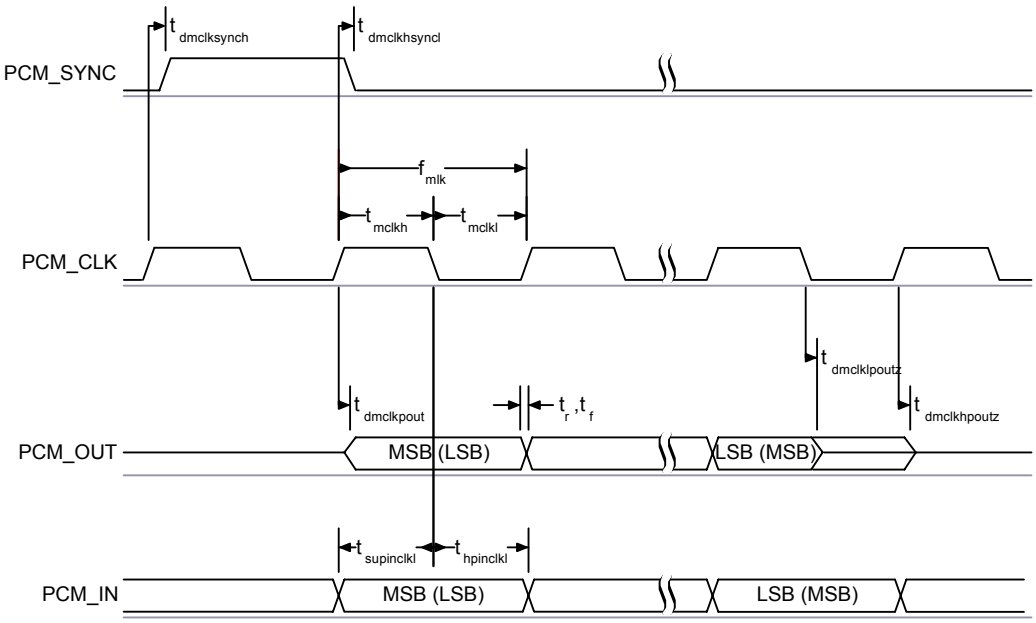


Figure 9.24: PCM Master Timing Short Frame Sync

Symbol	Parameter	Min	Typ	Max	Unit
f_{sclk}	PCM clock frequency (Slave mode: input)	64	-	2048	kHz
f_{sclk}	PCM clock frequency (GCI mode)	128	-	4096	kHz
t_{sclkl}	PCM_CLK low time	200	-	-	ns
t_{sclkh}	PCM_CLK high time	200	-	-	ns
$t_{hsclksynch}$	Hold time from PCM_CLK low to PCM_SYNC high	30	-	-	ns
$t_{susclksynch}$	Set-up time for PCM_SYNC high to PCM_CLK low	30	-	-	ns
t_{dpout}	Delay time from PCM_SYNC or PCM_CLK whichever is later, to valid PCM_OUT data (Long Frame Sync only)	-	-	20	ns
$t_{dsclkhpout}$	Delay time from CLK high to PCM_OUT valid data	-	-	20	ns
t_{dpoutz}	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	20	ns
$t_{supinsclkl}$	Set-up time for PCM_IN valid to CLK low	30	-	-	ns
$t_{hpinsclkl}$	Hold time for PCM_CLK low to PCM_IN invalid	30	-	-	ns

Table 9.10: PCM Slave Timing

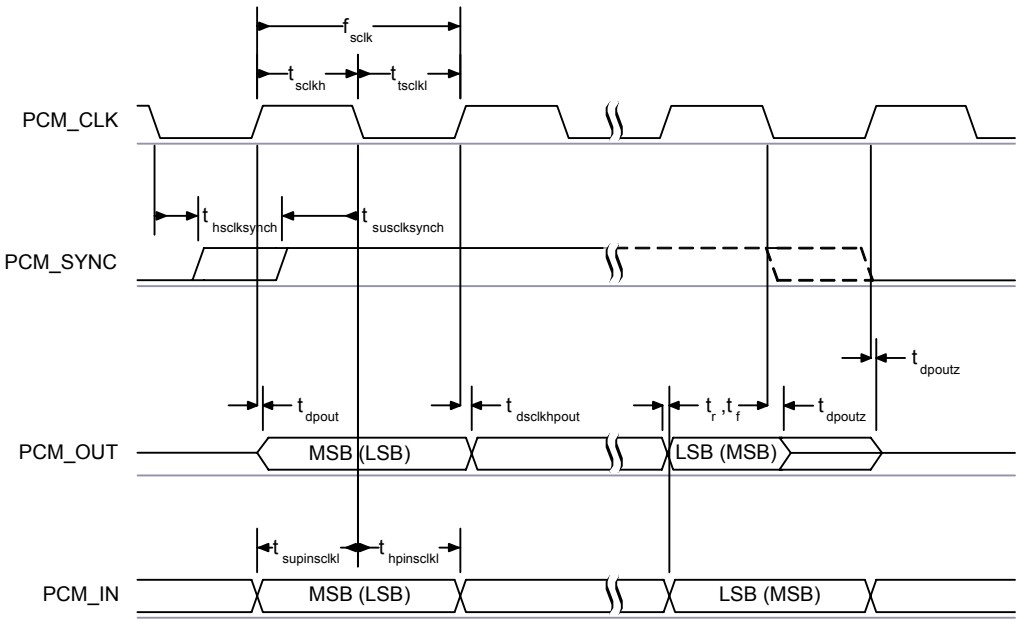


Figure 9.25: PCM Slave Timing Long Frame Sync

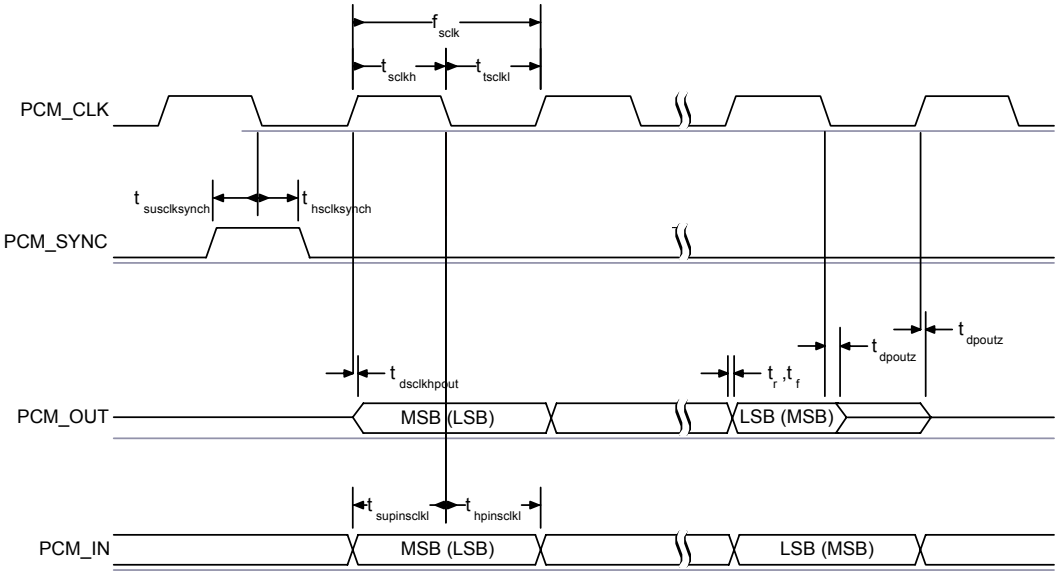


Figure 9.26: PCM Slave Timing Short Frame Sync

PCM_CLK and PCM_SYNC Generation

BlueCore4-ROM has two methods of generating PCM_CLK and PCM_SYNC in master mode. The first is generating these signals by *Direct Digital Synthesis* (DDS) from BlueCore4-ROM internal 4MHz clock (which is used in BlueCore2-External). Using this mode limits PCM_CLK to 128, 256 or 512kHz and PCM_SYNC to 8kHz. The second is generating PCM_CLK and PCM_SYNC by DDS from an internal 48MHz clock (which allows a greater range of frequencies to be generated with low jitter but consumes more power). This second method is selected by setting bit 48M_PCM_CLK_GEN_EN in PSKEY_PCM_CONFIG32. When in this mode and with long frame sync, the length of PCM_SYNC can be either 8 or 16 cycles of PCM_CLK, determined by LONG_LENGTH_SYNC_EN in PSKEY_PCM_CONFIG32.

The Equation 9.11 describes PCM_CLK frequency when being generated using the internal 48MHz clock:

$$f = \frac{CNT\_RATE}{CNT\_LIMIT} \times 24MHz$$

Equation 9.11: PCM_CLK Frequency When Being Generated Using the Internal 48MHz Clock

The frequency of PCM_SYNC relative to PCM_CLK can be set using Equation 9.12:

$$f = \frac{PCM\_CLK}{SYNC\_LIMIT \times 8}$$

Equation 9.12: PCM_SYNC Frequency Relative to PCM_CLK

CNT_RATE, CNT_LIMIT and SYNC_LIMIT are set using PSKEY_PCM_LOW_JITTER_CONFIG. As an example, to generate PCM_CLK at 512kHz with PCM_SYNC at 8kHz, set PSKEY_PCM_LOW_JITTER_CONFIG to `0x08080177`.

9.7.9 PCM Configuration

The PCM configuration is set using two PS Keys, PSKEY_PCM_CONFIG32 detailed in Table 9.11 and PSKEY_PCM_LOW_JITTER_CONFIG in Table 9.12. The default for PSKEY_PCM_CONFIG32 is `0x00800000`, i.e., first slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK from 4MHz internal clock with no tri-state of PCM_OUT.

Name	Bit Position	Description
-	0	Set to 0
SLAVE_MODE_EN	1	0 = master mode with internal generation of PCM_CLK and PCM_SYNC. 1 = slave mode requiring externally generated PCM_CLK and PCM_SYNC.
SHORT_SYNC_EN	2	0 = long frame sync (rising edge indicates start of frame). 1 = short frame sync (falling edge indicates start of frame).
-	3	Set to 0.
SIGN_EXTEND_EN	4	0 = padding of 8 or 13-bit voice sample into a 16-bit slot by inserting extra LSBs. When padding is selected with 13-bit voice sample, the 3 padding bits are the audio gain setting; with 8-bit sample the 8 padding bits are zeroes. 1 = sign-extension.
LSB_FIRST_EN	5	0 = MSB first of transmit and receive voice samples. 1 = LSB first of transmit and receive voice samples.
TX_TRISTATE_EN	6	0 = drive PCM_OUT continuously. 1 = tri-state PCM_OUT immediately after falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is not active.
TX_TRISTATE_RISING_EDGE_EN	7	0 = tri-state PCM_OUT immediately after falling edge of PCM_CLK in last bit of an active slot, assuming the next slot is also not active. 1 = tri-state PCM_OUT after rising edge of PCM_CLK.
SYNC_SUPPRESS_EN	8	0 = enable PCM_SYNC output when master. 1 = suppress PCM_SYNC whilst keeping PCM_CLK running. Some CODECS utilise this to enter a low power state.
GCI_MODE_EN	9	1 = enable GCI mode
MUTE_EN	10	1 = force PCM_OUT to 0
48M_PCM_CLK_GEN_EN	11	0 = set PCM_CLK and PCM_SYNC generation via DDS from internal 4MHz clock. 1 = set PCM_CLK and PCM_SYNC generation via DDS from internal 48MHz clock.
LONG_LENGTH_SYNC_EN	12	0 = set PCM_SYNC length to 8 PCM_CLK cycles. 1 = set length to 16 PCM_CLK cycles. Only applies for long frame sync and with 48M_PCM_CLK_GEN_EN set to 1.
-	[20:16]	Set to `0b00000`
MASTER_CLK_RATE	[22:21]	Selects 128 (`0b01`), 256 (`0b00`), 512 (`0b10`) kHz PCM_CLK frequency when master and 48M_PCM_CLK_GEN_EN (bit 11) is low.
ACTIVE_SLOT	[26:23]	Default is `0001`. Ignored by firmware.

Name	Bit Position	Description
SAMPLE_FORMAT	[28:27]	Selects between 13 (0b00), 16 (0b01), 8 (0b10) bit sample with 16 cycle slot duration or 8 (0b11) bit sample with 8 cycle slot duration.

Table 9.11: PSKEY_PCM_CONFIG32 Description

Name	Bit Position	Description
CNT_LIMIT	[12:0]	Sets PCM_CLK counter limit
CNT_RATE	[23:16]	Sets PCM_CLK count rate
SYNC_LIMIT	[31:24]	Sets PCM_SYNC division relative to PCM_CLK

Table 9.12: PSKEY_PCM_LOW_JITTER_CONFIG Description

9.8 I/O Parallel Ports

Fifteen lines of programmable bi-directional input/outputs (I/O) are provided. PIO[11:8] and PIO[3:0] are powered from VDD_PIO. PIO[7:4] are powered from VDD_PADS. AIO [2:0] are powered from VDD_MEM.

PIO lines can be configured through software to have either weak or strong pull-ups or pull-downs. All PIO lines are configured as inputs with weak pull-downs at reset.

PIO[0] and PIO[1] are normally dedicated to RXEN and TXEN respectively, but they are available for general use.

Any of the PIO lines can be configured as interrupt request lines or as wake-up lines from sleep modes. PIO[6] or PIO[2] can be configured as a request line for an external clock source. This is useful when the clock to BlueCore4-ROM is provided from a system *application specific integrated circuit* (ASIC). Using PSKEY_CLOCK_REQUEST_ENABLE (0x246), this terminal can be configured to be low when BlueCore4-ROM is in Deep Sleep and high when a clock is required. The clock must be supplied within 4ms of the rising edge of PIO[6] or PIO[2] to avoid losing timing accuracy in certain Bluetooth operating modes.

BlueCore4-ROM has three general purpose analogue interface pins, AIO[0], AIO[1] and AIO[2]. These are used to access internal circuitry and control signals. One pin is allocated to decoupling for the on-chip band gap reference voltage, the other two may be configured to provide additional functionality.

9.8.1 PIO Defaults

CSR cannot guarantee that these terminal functions remain the same. Refer to the software release note for the implementation of these PIO lines, as they are firmware build-specific.

9.9 I/O Functionality for 802.11 (Wi-Fi) Coexistence Schemes

PIO4, PIO5, PIO6, PIO7 and PIO9 can be used to implement a variety of 3 and 4-wire 802.11 (Wi-Fi) coexistence schemes, and other PIOs can be configured to do so. Channel skipping AFH, priority signalling, channel signalling and host passing of channel instructions are all supported. For further details, contact CSR.

PIO	Ball	Signal Name/Coexistence Functionality
PIO[9]	C3	WLAN_ACTIVE [a]
PIO[7]	F9	RF_ACTIVE
PIO[6]	F10	WLAN_ACTIVE [a]
PIO[5]	F8	BT_STATUS
PIO[4]	E8	BT_PRIORITY [a]

Table 9.13: I/O Functionality for 802.11 (Wi-Fi) Coexistence Schemes

[a] The coexistence functionality of this PIO can be assigned to another PIO using CSR's PS Keys.

9.10 I²C Interface

PIO[8:6] can be used to form a master I²C interface. The interface is formed using software to drive these lines. Therefore, it is suited only to relatively slow functions such as driving a dot matrix *liquid crystal display* (LCD), keyboard scanner or EEPROM.

Any three PIOs can be used as a master I²C interface by configuring the hardware bit serialiser with suitable firmware. The strong pull-ups in the PIO pads eliminate the need for external pull-up resistors.

Notes:

PIO lines need to be pulled-up through 2.2kΩ resistors.

PIO[7:6] dual functions, UART bypass and EEPROM support, therefore, devices using an EEPROM cannot support UART bypass mode.

For connection to EEPROMs, refer to CSR documentation on I²C EEPROMs for use with BlueCore. This provides information on the type of devices currently supported.

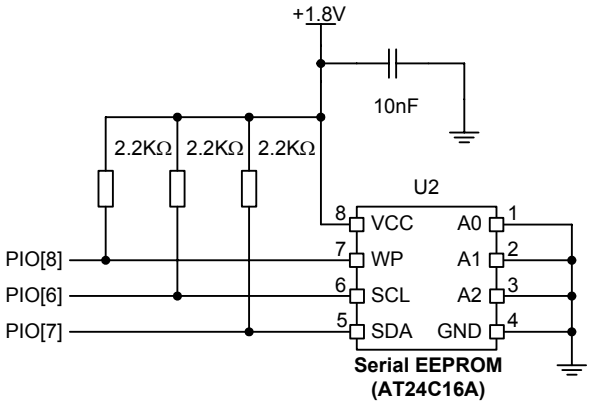


Figure 9.27: Example EEPROM Connection

9.11 TCXO Enable OR Function

An OR function exists for clock enable signals from a host controller and BlueCore4-ROM where either device can turn on the clock without having to wake up the other device. PIO[3] can be used as the host clock enables input and PIO[2] can be used as the OR output with the TCXO enable signal from BlueCore4-ROM.

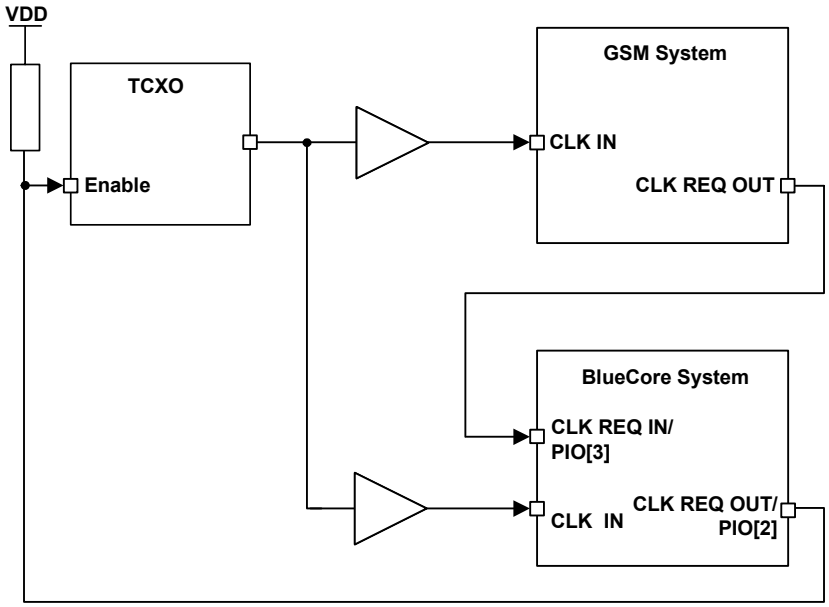


Figure 9.28: Example TCXO Enable OR Function

On reset and up to the time the PIO has been configured, PIO[2] will be tri-state. Therefore, the developer must ensure that the circuitry connected to this pin is pulled via a 470kΩ resistor to the appropriate power rail. This ensures that the TCXO is oscillating at start up.

9.12 RESET and RESETB

BlueCore4-ROM may be reset from several sources:

- RESET or RESETB pins
- Power on reset
- A UART break character
- Via a software configured watchdog timer

The RESET pin is an active high reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5ms and 4.0ms following RESET being active. It is recommended that RESET be applied for a period greater than 5ms. The RESETB pin is the active low version of RESET and is OR'd on-chip with the active high RESET, with either causing the reset function.

The power on reset occurs when the VDD_CORE supply falls below typically 1.5V and is released when VDD_CORE rises above typically 1.6V.

At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-state. The PIOs have weak pull-downs.

Following a reset, BlueCore4-ROM assumes the maximum XTAL_IN frequency, which ensures that the internal clocks run at a safe (low) frequency until BlueCore4-ROM is configured for the actual XTAL_IN frequency. If no clock is present at XTAL_IN, the oscillator in BlueCore4-ROM free runs, again at a safe frequency.

9.12.1 Pin States on Reset

Table 9.14 shows the pin states of BlueCore4-ROM on reset.

Pin Name	State: BlueCore4-ROM
PIO[11:0]	Input with weak pull-down
PCM_OUT	Tri-state with weak pull-down
PCM_IN	Input with weak pull-down
PCM_SYNC	Input with weak pull-down
PCM_CLK	Input with weak pull-down
UART_TX	Output tri-state with weak pull-up
UART_RX	Input with weak pull-down
UART_RTS	Output tri-state with weak pull-up
UART_CTS	Input with weak pull-down
USB_DP	Input with weak pull-down
USB_DN	Input with weak pull-down
SPI_CSB	Input with weak pull-up
SPI_CLK	Input with weak pull-down
SPI_MOSI	Input with weak pull-down
SPI_MISO	Output tri-state with weak pull-down
AIO[2:0]	Output, driving low
RESET	Input with weak pull-down
RESETB	Input with weak pull-up
TEST_EN	Input with strong pull-down
AUX_DAC	High impedance
TX_A	High impedance
TX_B	High impedance
RF_IN	High impedance
XTAL_IN	High impedance, 250k to XTAL_OUT
XTAL_OUT	High impedance, 250k to XTAL_IN

Table 9.14: Pin States of BlueCore4-ROM on Reset

9.12.2 Status after Reset

The chip status after a reset is as follows:

- Warm Reset: Data Rate and RAM data remain available
- Cold Reset(1) : Data Rate and RAM data not available

(1) A Cold Reset is either Power cycle, system reset (firmware fault code) or Reset signal. See .

9.13 Power Supply

9.13.1 1.8V Power Supplies

BlueCore4-ROM contains a 1.8V regulator which may be used to power the 1.8V supplies of the device. The device pin VREG_EN is used to enable and disable the regulator. Alternatively, an external 1.8V voltage source may be used.

9.13.2 Sequencing

The 1.8V supplies are VDD_ANA, VDD_VCO, VDD_RADIO and VDD_CORE. It is recommended that the 1.8V supplies are all powered at the same time. The order of powering the 1.8V supplies relative to the other IO supplies (VDD_PIO, VDD_PADS, VDD_USB) is not important. However, if the IO supplies are powered before the 1.8V supplies all digital IO will have a weak pull-down irrespective of the reset state.

9.13.3 External Voltage Source

If the 1.8V rails of BlueCore4-ROM are supplied from an external voltage source, it is recommended that , VDD_RADIO, and VDD_ANA, should have less than 10mV rms noise levels between 0 to 10MHz.

Single tone frequencies are also to be avoided. The transient response of any regulator used should be 20µs or less. It is essential that the power rail recovers quickly at the start of a packet, where the power consumption will jump to high levels (see average current consumption section).

9.13.4 Voltage Regulator

An on-chip linear voltage regulator can be used to power the 1.8V dependent supplies. It is advised that a smoothing circuit using a 2.2µF low ESR capacitor and 2.2Ω resistor be placed on the output VDD_ANA adjacent to VREG_IN.

The regulator is switched into a low power mode when the device is sent into Deep Sleep mode. When the on-chip regulator is not required VDD_ANA is a 1.8V input and VREG_IN must be either open circuit or tied to VDD_ANA.

9.13.5 VREG_EN Pin

The regulator enable pin, VREG_EN, can be used to enable and disable the BlueCore4-ROM device if the on-chip regulator is being used. The pin is active high and has an internal weak pull-up to enable the regulator if VREG_EN is not connected.

10 Example Application Schematic

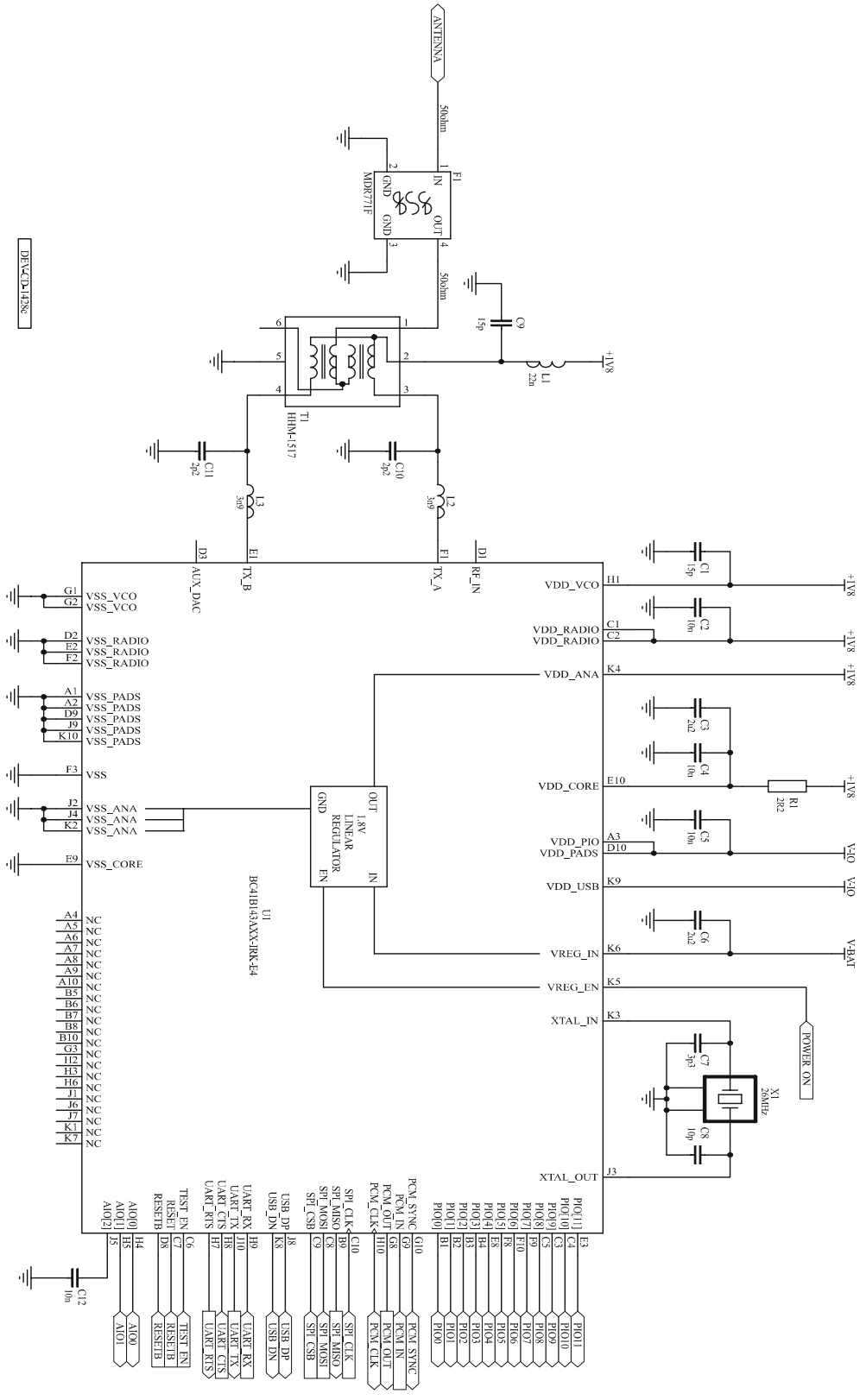
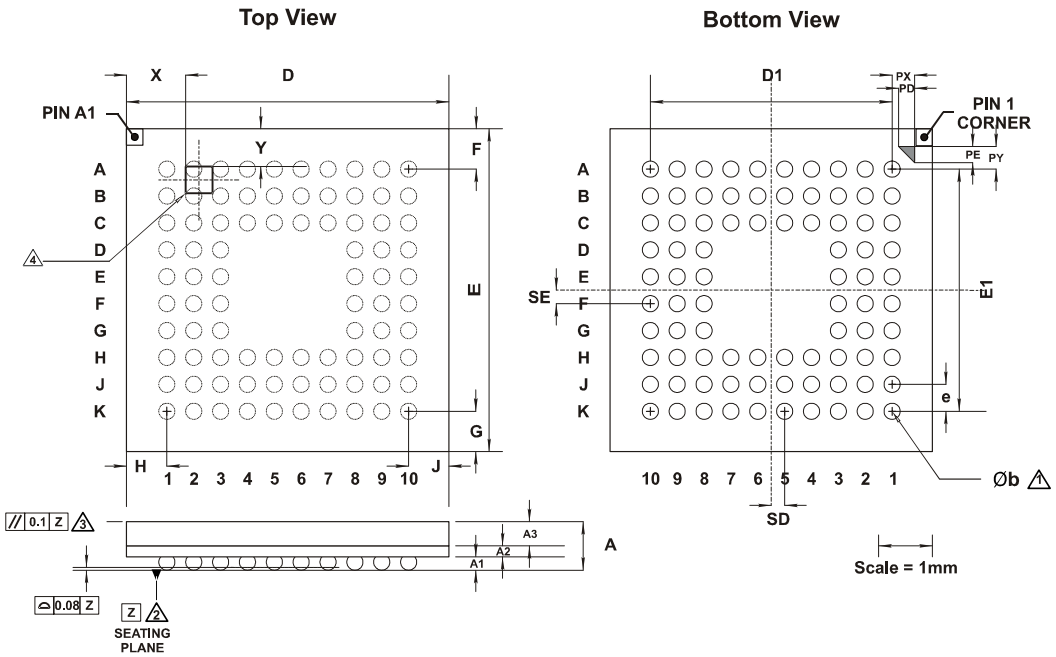


Figure 10.1: Example Application Circuit for Radio Characteristics Specification

11 Package Dimensions



Description	84-Ball Very-Thin Fine-Pitch Ball Grid Array (VFBGA)			
Size	6 x 6 x 1mm			
Pitch	0.5mm			
Dimension	**Minimum**	**Typical**	**Maximum**	**Notes**
A	0.8	0.9	1.0	(1) Dimension b is measured at the maximum solder ball diameter parallel to datum plane Z
A1	0.2	0.25	0.3	
A2		0.22		
A3		0.45		
b	0.25	0.30	0.35	(2) Datum Z is defined by the spherical crowns of the solder balls
D	5.90	6.00	6.10	
E	5.90	6.00	6.10	
e		0.50		(3) Parallelism measurement shall exclude any effect of mark on top surface of package
D1		4.50		
E1		4.50		
F	0.700	0.750	0.800	
G	0.700	0.750	0.800	(4) Polarity Mark. The dimensions of the polarity mark are 0.5 x 0.5mm.
H	0.700	0.750	0.800	
J	0.700	0.750	0.800	
PD		0.300		
PX		0.420		
PE		0.300		
PY		0.420		
SD		0.25		
SE		0.25		
X		1.10		
Y		0.70		
JEDEC	MO-225			
Unit	mm			

Figure 11.1: BlueCore4-ROM BGA Package Dimensions

12 PCB Design and Assembly Considerations

12.1 6 x 6mm VFBGA 84-Ball Package

This section lists recommendations to achieve maximum board-level reliability of the 6 x 6mm VFBGA 84-ball package:

- *Non solder mask defined* (NSMD) lands (that is, lands smaller than the solder mask aperture) are preferred because of the greater accuracy of the metal definition process compared to the solder mask process. With solder mask defined pads, the overlap of the solder mask on the land creates a step in the solder at the land interface, which can cause stress concentration and act as a point for crack initiation.
- Ideally, via-in-pad technology should be used to achieve truly NSMD lands. Where this is not possible, a maximum of one trace connected to each land is preferred and this trace should be as thin as possible – taking into consideration its current carrying and the radio frequency (RF) requirements.
- 35µm thick (1oz) copper lands are recommended rather than 17µm thick (0.5oz). This results in a greater standoff which has been proven to provide greater reliability during thermal cycling.
- Land diameter should be the same as that on the package to achieve optimum reliability.
- Solder paste is preferred to flux during the assembly process because this adds to the final volume of solder in the joint, increasing its reliability.
- Where a nickel gold plating finish is used, the gold thickness should be kept below 0.5µm to prevent brittle gold/tin intermetallics forming in the solder.

13 Solder Profiles

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder re-flow. There are four zones:

1. **Preheat Zone** - This zone raises the temperature at a controlled rate, typically 1-2.5°C/s.
2. **Equilibrium Zone** - This zone brings the board to a uniform temperature and also activates the flux. The duration in this zone (typically 2-3 minutes) will need to be adjusted to optimise the out gassing of the flux.
3. **Reflow Zone** - The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint.
4. **Cooling Zone** - The cooling rate should be fast, to keep the solder grains small which will give a longer lasting joint. Typical rates will be 2-5°C/s.

13.1 Typical Solder Re-flow Profile for Devices with Lead-Free Solder Balls

Composition of the solder ball:Sn 95.5%, Ag 4.0%, Cu 0.5%

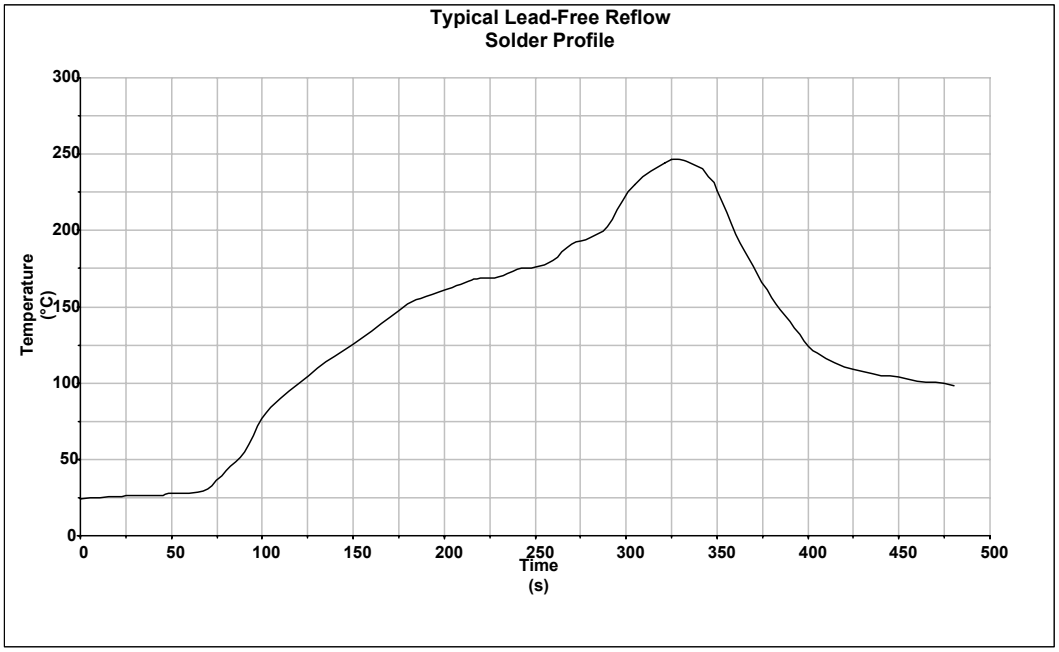


Figure 13.1: Typical Lead-Free Re-flow Solder Profile

Key features of the profile:

- Initial Ramp = 1-2.5°C/sec to 175°C±25°C equilibrium
- Equilibrium time = 60 to 180 seconds
- Ramp to Maximum temperature (245°C) = 3°C/sec max.
- Time above liquidus temperature (217°C): 45-90 seconds
- Device absolute maximum reflow temperature: 260°C

Devices will withstand the specified profile.

Lead-free devices will withstand up to three reflows to a maximum temperature of 260°C.

14 RoHS Statement with a List of Banned Materials

14.1 RoHS Statement

BlueCore4-ROM where explicitly stated in this Data Sheet meets the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS).

14.1.1 List of Banned Materials

The following banned substances are not present in BlueCore4-ROM which is compliant with RoHS:

- Cadmium
- Lead
- Mercury
- Hexavalent chromium
- PBB (Polybrominated Bi-Phenyl)
- PBDE (Polybrominated Diphenyl Ether)

In addition, BlueCore4-ROM is free from the following substances:

- PVC (Polyvinyl Chloride)

15 Ordering Information

15.1 BlueCore4-ROM

Interface Version	Package			Order Number
	Type	Size	Shipment Method	
UART and USB	84-Ball VFBGA (Pb free)	6 x 6 x 1mm	Tape and reel	BC41B143A07-IRK-E4

Minimum Order Quantity

2kpcs taped and reeled

To contact a CSR representative, email sales@csr.com or go to www.csr.com/contacts.htm.

For tape and reel packing and labelling information, see the *IC Packing and Labelling Specification*.

16 Document References

Document	Reference
Specification of the Bluetooth System	v2.1 + EDR, 26 July 2007
Specification of the Bluetooth System	v2.0 + EDR, 10 November 2004
Universal Serial Bus Specification	v2.0, 27 April 2000
Selection of I²C EEPROMS for Use with BlueCore	bcore-an-008Pb, 30 September 2003
EDR RF Test Specification v2.0.E.2	v2.0.E.2, 04 November 2004
IC Packing and Labelling Specification	CS-112584-SPP1, January 2007

17 Terms and Definitions

8DPSK	8 phase Differential Phase Shift Keying
π/4 DQPSK	pi/4 rotated Differential Quaternary Phase Shift Keying
AC	Alternating Current
ACL	Asynchronous Connection-Less, a Bluetooth data packet type
ADC	Analogue to Digital Converter
AFH	Adaptive Frequency Hopping
AGC	Automatic Gain Control
A-law	Audio encoding standard
BCCMD	BlueCore Command
BCHS	BlueCore Host Software
BCSP	BlueCore™ Serial Protocol
BER	Bit Error Rate. Used to measure the quality of a link
BGA	Ball Grid Array
BIST	Built-In Self-Test
BlueCore™	Group term for CSR's range of Bluetooth chips
Bluetooth™	Set of technologies providing audio and data transfer over short-range radio connections
BMC	Burst Mode Controller
C/I	Carrier Over Interferer
CDMA	Code Division Multiple Access
CMOS	Complementary Metal Oxide Semiconductor
CODEC	Coder Decoder
CQDDR	Channel Quality Driven Data Rate
CRC	Cyclic Redundancy Check
CSB	Chip Select (Active Low)
CSR	Cambridge Silicon Radio
CVSD	Continuous Variable Slope Delta Modulation
DAC	Digital to Analogue Converter
dBm	Decibels relative to 1mW
DC	Direct Current
DEVM	Differential Error Vector Magnitude
EDR	Enhanced Data Rate
EEPROM	Electrically Erasable Programmable Read Only Memory
eSCO	Extended Synchronous Connection-Orientated
ESR	Equivalent Series Resistance
FSK	Frequency Shift Keying
GSM	Global System for Mobile communications
HCI	Host Controller Interface

HV	Header Value
I/O	Input Output
IF	Intermediate Frequency
IQ Modulation	In-Phase and Quadrature Modulation
ISDN	Integrated Services Digital Network
ISM	Industrial, Scientific and Medical
ksamples/s	KiloSamples Per Second
L2CAP	Logical Link Control and Adaptation Protocol (protocol layer)
LC	Link Controller
LED	Light Emitting Diode
LMP	Link Manager Protocol
LNA	Low Noise Amplifier
LSB	Least-Significant Bit
MCU	MicroController Unit
MMU	Memory Management Unit
MISO	Master In Serial Out
MOSI	Master Out Slave In
μ-law	Audio Encoding Standard
OHCI	Open Host Controller Interface
PA	Power Amplifier
PCB	Printed Circuit Board
PCM	Pulse Code Modulation. Refers to digital voice data
PDA	Personal Digital Assistant
PICS	Protocol Implementation Conformance Statement
PIO	Parallel Input Output
ppm	parts per million
PS Key	Persistent Store Key
RAM	Random Access Memory
RF	Radio Frequency
RISC	Reduced Instruction Set Computer
rms	root mean squared
RoHS	The Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive (2002/95/EC)
ROM	Read Only Memory
RSSI	Receive Signal Strength Indication
RTS	Ready To Send
RX	Receive or Receiver
SCO	Synchronous Connection-Oriented. Voice oriented Bluetooth packet
SDK	Software Development Kit
SDP	Service Discovery Protocol

SPI	Serial Peripheral Interface
SSI	Synchronous Serial Interface
TBA	To Be Announced
TBD	To Be Defined
TCXO	Temperature Controlled crystal Oscillator
TDMA	Time Division Multiple Access
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
UHCI	Upper Host Control Interface
USB	Universal Serial Bus or Upper Side Band (depending on context)
VCO	Voltage Controlled Oscillator
VFBGA	Very Fine Ball Grid Array
W-CDMA	Wideband Code Division Multiple Access
WEB	Write Enable (Active Low)
WLAN	Wireless Local Area Network
www	world wide web

18 Document History

Revision	Date	History
a	FEB 05	Original publication of this document. (CSR reference: BC41B143A-ds-001Pa)
b	MAR 05	Update to section 2 (Key Features) and section 3.2 (UART_RX and UART_CTS). CSR reference now BC41B143A-ds-002Pb.
c	AUG 05	Updated Auxiliary DAC in Description of Functional Blocks Amendment to notes in Electrical Characteristics concerning ▪ specified output voltage in the Auxiliary DAC table ▪ VREG_EN and VREG_IN in Linear Regulator table Power Consumption moved from Radio Characteristics - Basic Data Rate to Electrical Characteristics. Editorial and copyright updates
d	SEPT 05	Data sheet raised to Production status. Major changes include updated Radio Characteristics (Basic Data Rate and EDR) and the addition of Typical Radio Performance - Basic Data Rate
e	DEC 05	Tape and Reel Information, Solder Profiles, PCB Design and Assembly Considerations sections and RoHS Statement added to the Data Book; Clock Start Up Delay updated in Device Terminal Descriptions, XTAL_IN
f	FEB 06	Tape and Reel Information and Solder Profiles updated in Data Book.
g	MAR 06	Corrections made to Power Supplies and Control table in Device Terminal Functions section of Package Information
h	APR 06	Correction made to Serial Synchronous Interface, Description of Functional Blocks
9	JAN 07	New CSR reference (CS-101564-DSP9); Application Schematic updated; missing table notes restored to Radio Characteristics - Basic Data Rate; Tape and Reel Information now referenced from Ordering Information; minor textual edits
10	JAN 07	Device Features updated; Ordering information updated
11	APR 07	Typical Radio Performance section removed from Data Sheet in line with CSR documentation standards (Data Book remains unchanged)
12	NOV 07	Product/Order number updated. References to Bluetooth specification updated

BlueCore™4-ROM
Product Data Sheet
CS-101564-DSP12
November 2007